DESIGN AND SIMULATION OF E-MODE GaN HEMTs FOR PORTABLE POWER CONVERTERS IN ELECTRIC VECHICLES

A Project report submitted in partial fulfilment of the requirements for

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IN
ELECTRONICS AND COMMUNICATION ENGINEERING

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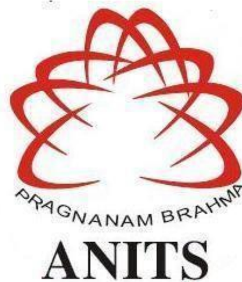

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY AND SCIENCES

(UGC AUTONOMOUS)

(*Permanently Affiliated to AU, Approved by AICTE and Accredited by NBA & NAAC*)

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CERTIFICATE

This is to certify that the project report entitled **"DESIGN AND SIMULATION OF E-MODE GAN HEMTS FOR PORTABLE POWER CONVERTERS IN ELECTRIC VEHICLES"** submitted by **N. Sai Rohit (319126512100), P. VVSS Bhagavan (319126512110), D. Tejaswini (320126512L10), B. Eswara Rao (319126512073)** in partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology** in **Electronics & Communication Engineering** of Anil Neerukonda Institute of technology and Sciences(A), Visakhapatnam is a record of bonafide work carried out under my guidance and supervision.

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ABSTRACT

The Indian Electric Vehicle (EV) Industry is gradually gaining traction thanks to government initiatives. However, a widespread switch from internal combustion engine (ICE) vehicles to electric vehicles (EVs) necessitates the growth of infrastructure facilities, such as charging stations, and vehicles that might have a longer range (KM range with a single charge). The goal of a 100% EV adoption rate by 2030 should be achieved thanks to several government programs that boost the production and use of electric vehicles in the nation. Fossil fuels are used in internal combustion engines to power most automobiles now on the road. Due to the limited supply of fossil fuels and the carbon dioxide (CO_2) that is produced when these fuels react with air, the current transportation system is neither ecologically benign nor sustainable. Transportation applications are going toward electrification or increased electrification as a result of rising fuel prices and environmentally hazardous emissions. Because of the improved performance, decreased hazardous emissions, and enhanced efficiency that these applications offer, transportation electrification is particularly interesting. The greenhouse emissions impacts on global warming can be considerably reduced by electric vehicles (EV). The efficiency of the EV depends on the electric energy storage system (EESS), power converters, and motor drivers.

Silicon based diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) based power systems are experiencing more power loss during power conversion. The efficiency of the power converters can be improved by choosing suitable semiconductor devices which have low switching loss and conductions losses. Therefore, power devices used in EV must be extremely efficient, robust and power dense. Existing Si based power devices have low thermal dissipation and switching low frequency. To overcome the low switching efficiency and thermal properties of Si based devices, other semiconductors should be utilized. Benefits of WBG devices are acknowledged as these devices' size, weight, efficiency, and power density become more of a concern. High activation energy semiconductors are used in WBG devices. Compared to normal semiconductors, these semiconductors have a wider band gap. Higher switching rates are made possible by the large bandgap, which permits electrons to travel more quickly.

Depending on the Drain-Source voltage (V_{DS}), several types of preferred switches are employed in various applications. GaN devices are suitable for usage in power converters that operate at voltages between 100 V and 600 V. SiC is a suitable choice for voltages greater than 1200 V.

There are various obstacles to the adoption of electric vehicles, including limited charging infrastructure, size of the power converters, battery pack capacity, and cost. The aforementioned issues must be resolved in order to expand the number of EVs and meet the objectives set by the Indian government. In general, all type of Electric vehicles has a number of power electronics converters that are mostly used to run the motors of the batteries' motors and charge the batteries from the utility grid. For these power electronic converters, achieving high efficiency, robustness, small size, and low cost is a significant problem. The advantages of using GaN WBG devices in automotive industry are i) Enhancement mode GaN-HEMT up to 650 V ii) ten times better performance than Si iii) high current rating.

In view of the above, the main objective behind this project is to design and simulate Enhancement mode p-GaN gate HEMTs for low loss portable power converters in next generation electric vehicles.

Keywords: GaN HEMTs; Power converters; E-vehicle; Enhancement mode.

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CHAPTER 1

INTRODUCTION

This chapter fully discusses the distinctive features of GaN built materials in compared to other semiconductor substance. As a consequence, it will be evident why this particular material system was and remains to be the object of considerable study for over a decade now.

1.1 NITRIDE BASED SEMICONDCUTORS

Over the last 20 to 30 years, nitride-based semiconductor technology has improved significantly due to extensive scientific work that has tackled critical challenges inhibiting its development, such as high-quality growth and p-type doping. [1][2]. Several fields have been encouraged by the superior material properties of nitride alloys, which has expanded the range of potential application areas as depicted in Figure 1.1.

Because of their wide range of potential energy band gaps ranging from 0.7 eV (InN) to 6.2 eV, nitride-based devices in optoelectronics provide a full solution for emission and detection from infrared to ultraviolet. (AlN).

The prototype GaN electroluminescent semiconductor was shown in 1971. [3]. GaN-based light-emitting diode (LED) were further enhanced in a surprising fashion [4][2], and Nichia Chemical Industry released the first commercial LEDs in 1993. Later, its usage was broadened to encompass optoelectronic applications [5][6]**.** GaN-based devices are essential in the electronics and telecommunications industries for both high speed and high-power applications.

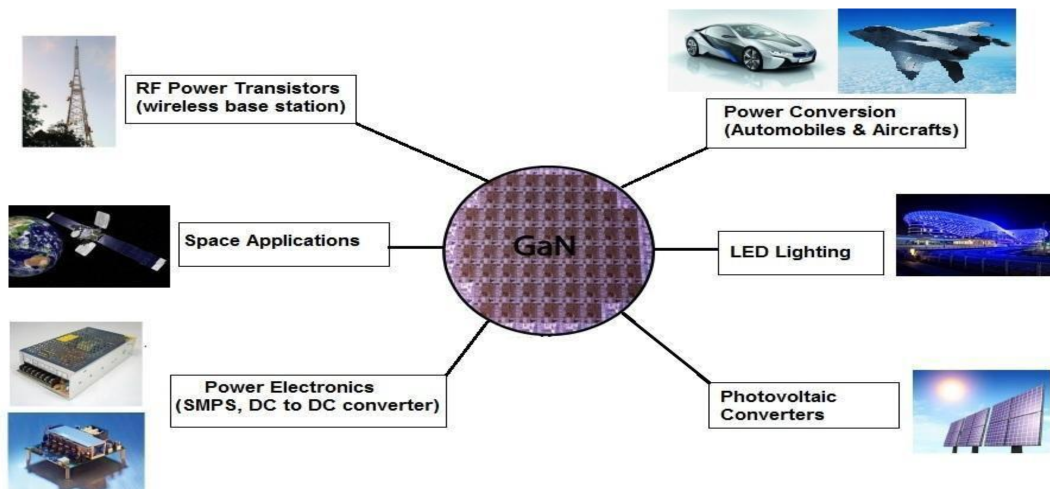

Fig. 1.1 Potential uses of GaN

Table 1.1 lists the essential electrical characteristics of every semiconductor material. Compared to all other types of material, including Si & GaAs, GaN has the largest electric breakdown field. Moreover, these GaN-based electron transistors are good choices for higher-frequency and high-power uses because of their highest saturation velocity and improved mobility.

Table 1.1 Semiconductor materials properties.

Material Properties	Si	GaAs	SiC	GaN	Diamond
Band gap $E_g(eV)$	1.1	1.4	3.3	3.4	5.5
Permittivity ε_r	11.8	13.1	10	9.0	5.5
Electron mobility $\mu_n(cm^2V^{-1}s^{-1})$	1350	8500	700	1200	1900
Saturation velocity $v_{sat}(10^7 cm/s)$	1.0	1.0	2.0	2.5	2.7
Critical electric field $E_{cr}(MV/cm)$	0.3	0.4	3.0	3.3	5.6
Thermal conductivity θ $(WK^{-1}m^{-1})$	150	43	330	130	2000
JFoM/JFoM$_{Si}$	1.0	1.3	20.0	27.5	50.4
BFoM/BFoM$_{Si}$	1.0	14.4	11.9	20.0	82.0

SiC's uses are limited despite having electrical properties that are comparable to those of GaN because of serious problems with heterojunction production and harsh processing conditions. Contrarily, the GaN material is simple to combine with other nitride alloys to generate heterojunctions, which makes it possible to create high electron mobility transistors (HEMTs), which have found applications in a variety of industries. Furthermore, the presence of polarisation-induced charge carriers (2DEG) at the heterojunction interface allows for quick and easy device fabrication because the 2DEG's high sheet charge density may be employed without external doping. Because of its important properties, GaN material has been widely used in electronics over the last three decades.

1.1.1 GAN-BASED TRANSISTOR

Since the initial GaN-based MESFET was published in 1993 [7], other major investigations have been undertaken to prove the presence of 2DEG with higher mobility by employing AlGaN/GaN HEMT design [8][9][10]. Hence, the GaN-based devices' basic framework resembles the HEMT design [7]. GaN-based transistors were suggested for high-

powered switching and high-power radio frequency (RF) uses because to their unusual qualities of both a large electric breakdown field as well as high mobility.
The typical breakdown voltage for powerful switching applications spans from 10 to 1000 V, whereas the frequency range that can be operated varies from kHz to MHz. High power RF applications at the same time in which the device provides the largest amounts of power while working at high frequencies, are another key usage of GaN-based transistors. The device's breakdown voltage and the electron's saturation velocity in the 2DEG are related to its capacity to handle high power and operate at high frequencies. As a result, semiconductors based on GaN will increasingly be used in high-power microwave applications.

1.2 BASIC PROPERTIES OF III-NITRIDE SEMICONDUCTORS

Binary (AlN, GaN, & InN) compound material is the main classification of the III-N compound semiconductors. $Al_xGa_{(1-x)}N$, $In_xAl_{(1-x)}N$, & $In_xGa_{(1-x)}N$ are ternary compound materials. $In_xAl_{(1-x)}Ga_{(1-x-y)}N$ is a quaternary alloy. All of the nitride substances are intriguing, however the only one that can be manufactured in fine standards on Sapphire, SiC, and/or Si substrate is GaN. This is the major rationale for adopting GaN materials in nitride-based technologies across a broad variety of applications, namely RF power devices, higher - frequency MMICs, laser and light emitting diodes, MEMS, and power converters. Gallium Nitride, on the contrary , doesn't quite create the systems on its own. AlN, AlGaN, InGaN, and InAlGaN are indeed the materials used to produce heterostructures for operational electronics and optoelectronics. In this part, we focus into III-N semiconductor, which are more useful to electrical devices.

With the exception of InAlN, the III-nitrides have greater band gaps and smaller lattice parameters than all the other III-V conventional semiconductor family like arsenides, phosphides, antimonides, & corresponding alloys. This is due to the fact that metal-nitrogen interactions are so strong. Table.1.2 includes the band gaps & lattice constants for binary nitride substances. Figure 1.2 illustrates the direct band gap and lattice parameter of nitride semiconductors alloy compared to those of various III-V semiconductor materials. The quadratic equation is followed by the energy band gaps of AlxGa(1-x)N, InxAl(1-x)N, and InxGa(1-x)N:

$$E_{g,A_xB_{1-x}N} = xE_{g,AN} + (1-x)E_{g,BN} - b_{ABN}x(1-x) \qquad (1.1)$$

Depending on the desired compound, A and B can be Al, Ga, or In, and b is the bending parameter. Table 1.2 provides the bowing parameters for the III-N family. Eg, binary nitride lattice constants a and c, and ternary nitride alloys' bending parameter b combined [11][12].

Table 1.2 Band gap and lattice constants of Nitrides and alloys

Material	Eg (eV)	a (A°)	c(A°)	Alloy	b(eV)
AlN	6.14	3.112	4.982	AlGaN	0.7
GaN	3.42	3.189	5.185	InGaN	1.4
InN	0.64	3.545	5.703	InAlN	5.36

III-nitrides differ from conventional III-V semiconductors in another way thanks to their crystal structure. The stable phase of III-nitride has a wurtzite structure, which is distinguished by hexagonal symmetry and the absence of an inversion center.

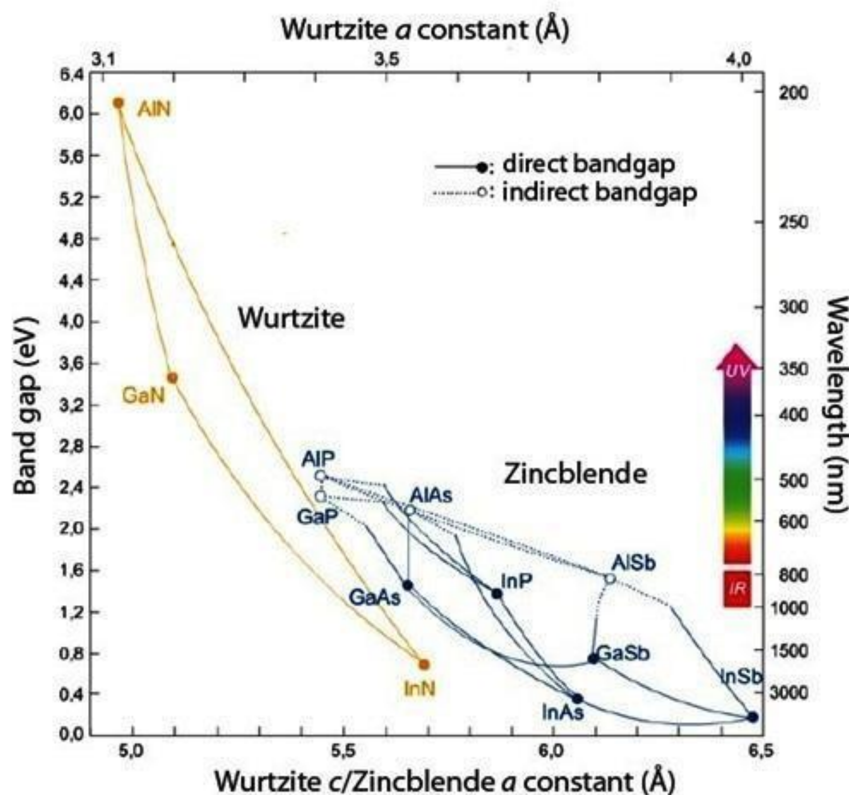

Fig. 1.2 shows the band gap of traditional zincblende III-V semiconductors and wurtzite III-nitrides as a function of lattice constants.

The basic wurtzite cell is represented in Figure 1.2, while typical III-Vs possess a more symmetrical cubic zincblende structure. The a and c parameters that characterize the crystalline structure of binary III-nitrides were provided in Table.1.2. The lattice parameter of all alloys may be readily calculated by linear interpolation of the appropriate binary compounds with no requirement for bending parameters. Since III-nitride devices & heterostructures are commonly formed along the x-axis, the parameter 'a', which is the lattice constant has become essential when addressing heterostructures.

1.3 ADVANTAGES OF III-N SEMICONDUCTOR

Nitrides are among the key semiconducting that have various features that make them desirable for usage in a number of electrical applications where compact, efficient devices are required to manage vast quantities of power. The breakdown voltage for III-nitride based systems is often larger than analogous devices with the same size made using Si or conventional III-Vs owing to the wide bandgap energy of GaN & III-nitride based alloys. Moreover, GaN has a greater saturation velocities than all the other semiconductors with wide band gaps like SiC, which enables parasitic resistors to be lowered and boosts the energy performance of the devices. Lastly, III-nitride semiconductors are particularly applicable for heterostructure-based devices. As a consequence, although this is not plausible for SiC and/or diamond-based systems, it is viable to test out band engineering to increase device efficiency in classical III-Vs, like through the induction of either quantum well (QW) and/or 2DEGs. GaN-based electron systems have largely found employment in two areas due to their properties: power electronic devices and microwave transistors. Table 1.1 provides merit figures for organic semiconductors from Johnson & Baliga [13]. The range of merits was reduced according to Si.

GaN has made it feasible to produce gadgets that have elevated breakdown voltage (V_{BR}) & extremely low specified on-resistance in the area of power electronic (R_{on}). Although a device handling high power densities requires a high breakdown strength (V_{BR}), a low Ron is necessary to limit energy loss in the ON-state. This same Baliga figure of merit (BFOM) [14] is indeed the merit figure that most properly gauges a semiconductor's capability for applications in power electronics:

$$BFOM = \epsilon \mu E_{BR}^{3} \quad (1.11)$$

Where E_{BR} is breakdown electric field , μ is the electron mobility when inside the drift zone, and ε is the semiconductor's dielectric constant. In line with how BFOM defines the ideal

trade-off between VBR and Ron, the following statement is more appropriate for comparing actual devices:

$$BFOM = \frac{V_{BR}^2}{R_{on}} \quad (1.12)$$

Table 1.1 lists the theoretical BFOM for the major semiconductors, and Figure 1.5 summarizes the VBR and Ron data for devices that have been reported (a) From this, it can be observed that GaN-based devices offer lower dissipation and lowered Ron both theoretically and practically. GaN-based vertical devices with relatively low ON- Resistances & Breakdown voltage levels as much as 1.5 kV were recorded, while increased performance of GaN-based P-N diode have been shown having 3.7kV Breakdown voltage [15]. [16]. This means that GaN has huge potential for medium- and low-voltage power devices and also is seriously being explored for enhancing the efficacy of DC to DC conversion [17] , LEDs [18] and motor drivers [19]etc.

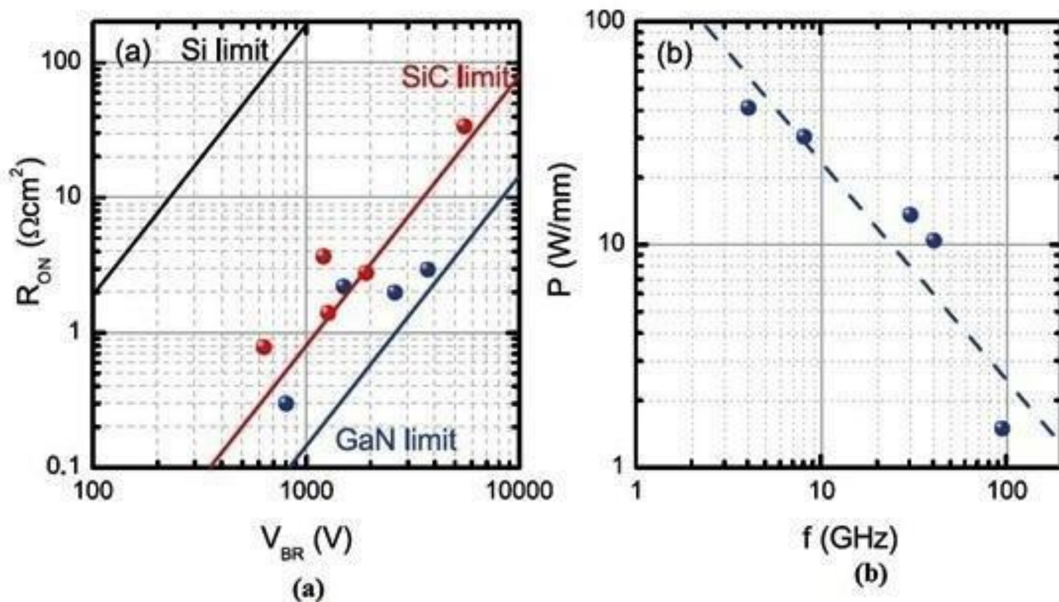

Fig. 1.3 (a) Lines: Theoretical restrictions of Si, SiC, and GaN. Dots: Particular ON-resistance versus. breakdown value for SiC [20][21][22][23]and GaN devices [15][16][18][24]. (a) Highest recorded power output densities of AlGaN/GaN HEMTs at different microwave frequencies [25] [26][27][28][29].

GaN is an intriguing material in microwave transistors, the goal of this study project, since it mixes a strong breakdown strength and a high related with coupled with relatively high electron velocity. A high breakdown level, especially in power electronics, is crucial for boosting a transistor's capacity to survive high power densities. Rather, a high saturation

velocities is recommended to shorten switching times by limiting the time required for electrons to pass across the base region or the gate electrode. By combining these two properties, GaN-based microwave transistor and amplifiers have the ability to generate extremely high output power levels while simultaneously having high cut-off frequencies. Johnson's merit scale is a method for assessing a material's feasibility for power microwave devices (JFoM)[30]:

$$JFoM = \frac{E_{BR}v_{sat}}{2\pi} \tag{1.13}$$

where V_{sat} is the saturation speed. The trade-off between V_{BR} and device speed is monitored by JFoM and expressed in terms its cut-off frequency f_T. Thus, the following definition is equal and appropriate for device comparison:

$$JFOM = V_{BR}f_T \tag{1.14}$$

The JFOM of semiconductors is mentioned in Table 1.1. As can be proven, GaN does have a tenfold greater JFOM over GaAs and is just exceeded by diamond. If we observe, diamond is expensive to dope and doesn't easily enable hetero-structures, hence GaN becomes the perfect material for RF applications. HEMTs with breakdown voltages much larger than that of III-V based HEMTs and/or bipolar transistor have been developed employing GaN-based heterostructures during the past 15 years[31]. This has led to record power outputs and efficiency for nitride based HEMTs, which are now commercially accessible for RF systems like cellular base stations that need high power levels.

1.4 BASIC HEMT STRUCTURE

Dingle et al. presented the HEMT's essential notion [32]. techniques describe how electrons migrate from a wide band gap semiconductor toward a tiny band gap material, generating a heterostructure with a triangular well at the interface that traps the electrons in 2DEG. This technique greatly lowers ionised impurity scattering by isolating the 2DEG from ionised donor that results in increased electron mobility & saturation velocity. Since the they is also identified by such a label, a HEMT is also called Modulation Doped Field Effect Transistor (MODFET). The term 2D-Electron-Gas Field Effect Transistor (TEGFET), that accentuates the 2DEG, is also relevant. Selectively Doped Heterojunction Transistor (SDHT), Separately Doped Field Effect Transistor (SEDFET), & Heterojunction Field Effect Transistor are alternate names for this technology. (HFET). The FET that emerges when the barrier layer, which is generally constructed from AlGaAs, is not doped is called a Heterostructure Insulated

Gate Field Effect Transistor (HIGFET) [33]. The first working HEMT was shown by [34]. AlGaN/GaN HEMT was first developed early 1994 by [35].

Field effect devices such as HEMTs employ 2DEG as its current channel. According to the basic field effect transistor architecture, these are composed of two ohmic contacts to the 2DEG, known as the drain and source contact, or a Schottky contact, known as the gate contact, lying in the drain-source gap. Figure 1.9 displays a vertical cross - sections of HEMT. The job of a electrode is to manage the current that flows through 2DEG between both the drain and source electrodes.

1.5 STATIC BEHAVIOUR

A current I_d flowing through two electrodes whenever a dc voltage is delivered to a drain electrode whereas the source electrode remains grounded. The amount of current I_d depends on the total resistivity of 2DEG channel. The gate electrode alters the channel's resistivity and consequently I_{ds} by changing the 2DEG density underneath it. The continuous current condition along the channel at a certain gate voltage Vgs will create its V-I characteristics, also known to as output characteristics.

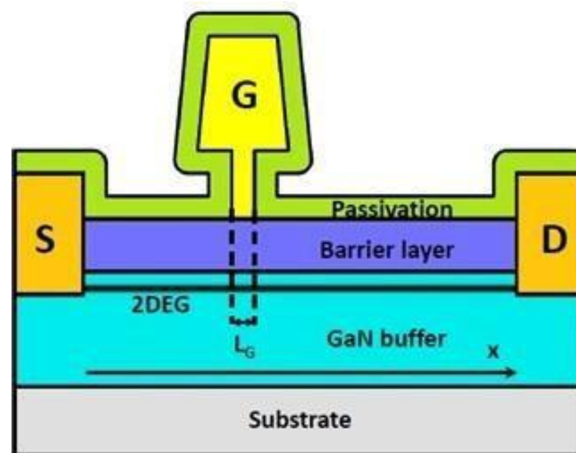

Fig. 1.4 Vertical cross section of III-nitride HEMT structure

Drain current Ids are influenced by sheet charge density ns, longitudinal electric field (E), and electron mobility (). the following is the phrase for Ids:

$$I_{ds} = wen(x)E(x)\mu \tag{1.15}$$

The device's gate length is W, and the sheet charge density n(x) in the gate region is plotted against the channel potential V(x) as follows:

$$n(x) = \frac{1}{e} C_b (V_{gs} - V(x) - V_{off}) \tag{1.16}$$

Considering $F(x) = \frac{dV(x)}{dx}$, Equation (1.19) can be written as:

$$I_{ds} = W\mu C_b \left(V_{gs} - V(x) - V_{off}\right) \frac{dV(x)}{dx} \tag{1.17}$$

Integrating this equation over the gate length, we finally obtain a relation between I_{ds} and V_{ds}:

$$I_{ds} = \frac{w\mu C_b}{2L_g}\left[\left(V_{gs} - V_{off}\right)^2 - \left(V_{gs} - V_{off} - V_{ds}\right)^2\right] \tag{1.18}$$

This expression is valid only for $V_{ds} < V_{gs} - V_{off}$ and for $V_{gs} > V_{off}$, i.e., in the linear region. When $V_{ds} = V_{gs} - V_{off}$ the whole channel at the drain edge is entirely depleted. In this scenario, the current doesn't quite grow more with V_{ds} and stays essentially constant. This constitutes the saturation region. Finally, for $V_{gs} < V_{off}$ the channel is totally depleted whatever V_{ds} and the device has reached the pinch-off state.

The V_{ds} Vs I_{ds} characteristics are illustrated in Figure 1.10 (a).

Figure 1.10 (b), which depicts $I_{ds} - V_{gs}$ dependency at a given V_{ds}, typically in saturation region, demonstrates the transfer characteristics of HEMTs. The following terms characterize the device's transconductance:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \text{ at constant } V_{ds} \tag{1.19}$$

Regarding the output characteristics, the V_{gs} dependency of gm in the saturation regime is typically depicted (Figure 1.10.b). Ids and gm both continue to rise with V_{gs} in a perfect HEMT. Yet, in actual devices, several nonlinearities help to alter the output and transfer characteristics.

1.6 ENHANCEMENT AND DEPLETION MODE HEMT

There are two types of HEMT structures available which can be manufactured for power application:

a. Enhancement Mode HEMT
b. Depletion Mode HEMT

Enhancement Mode will be the condition whereby the device only acts if a positive voltage being provided to it, while Depletion Mode is just the mode whereby the device performs regardless of whether a bias voltage has been applied, i.e., no extra potential is necessary to construct a channel across Source and Drain. Nevertheless, during Enhancement mode, a little

potential is necessary to first build a channel between both the drain and the source as for electrons to flow. This additional potential required creates the threshold voltage for Enhancement mode devices, which the applied potential must cross in order for current to pass through the device.

1.6.1 Why Enhancement Mode HEMT?

The enhancement mode HEMTs are simple to build, have a compact geometry, and dissipate little power. They are suitable for usage in integrated circuits due to these characteristics. When there is no voltage placed between the gate and source terminals, there is no route between the source and drain. The gate to source voltage boosts the channel in between, enabling current flow through it. This feature is what gives this component the designation "enhancement-mode HEMT”. Because there is no current flowing across source and drain when the device is switched off, the leakage current is very small, on the scale of nA. The power rail is typically connected to the HEMT's supply.

As a result, the amplification type gates are tunable within the HEMT’s power range. If the source is linked to the main power rail when using a depletion type HEMT, an auxiliary power supply is needed to reverse the gate bias. Since the enhanced HEMTs lack a predefined channel, they only permit current flow in the presence of a potent signal.

For all of these reasons, we choose an Enhancement Mode HEMT device over a Depletion Mode HEMT device.

CHAPTER 2

DEVICE PARAMETERS OF ENHANCEMENT MODE HEMT

In this chapter we discuss what parameters are crucial to check the credibility of an Enhancement Mode HEMT. We also try to understand what the parameters mean and what value of a particular parameter is required to check the device's credibility.

2.1 BAND DIAGRAM

The band diagrams of an E-Mode HEMT outlines the energy concentrations of the conduction band and valence band as well as the disparity in between two bands. This is a highly essential parameter since the bigger the energy gap between the bands of valence and conduction, the higher would be the electric field needed to break the device thereby boosting overall breakdown device voltage.

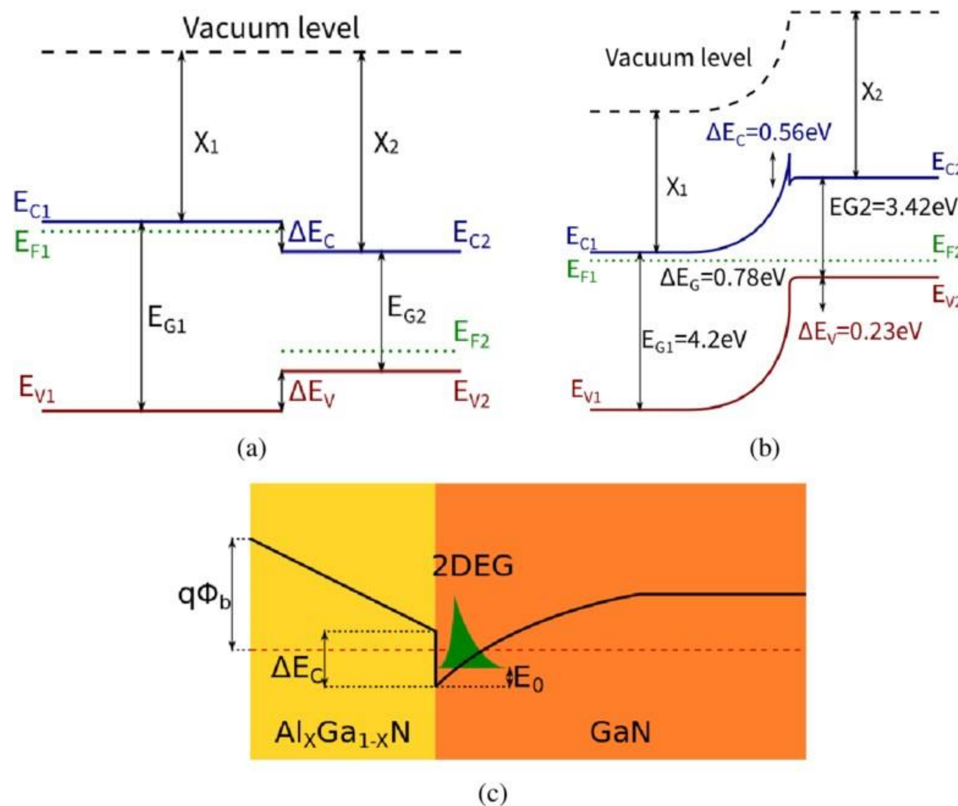

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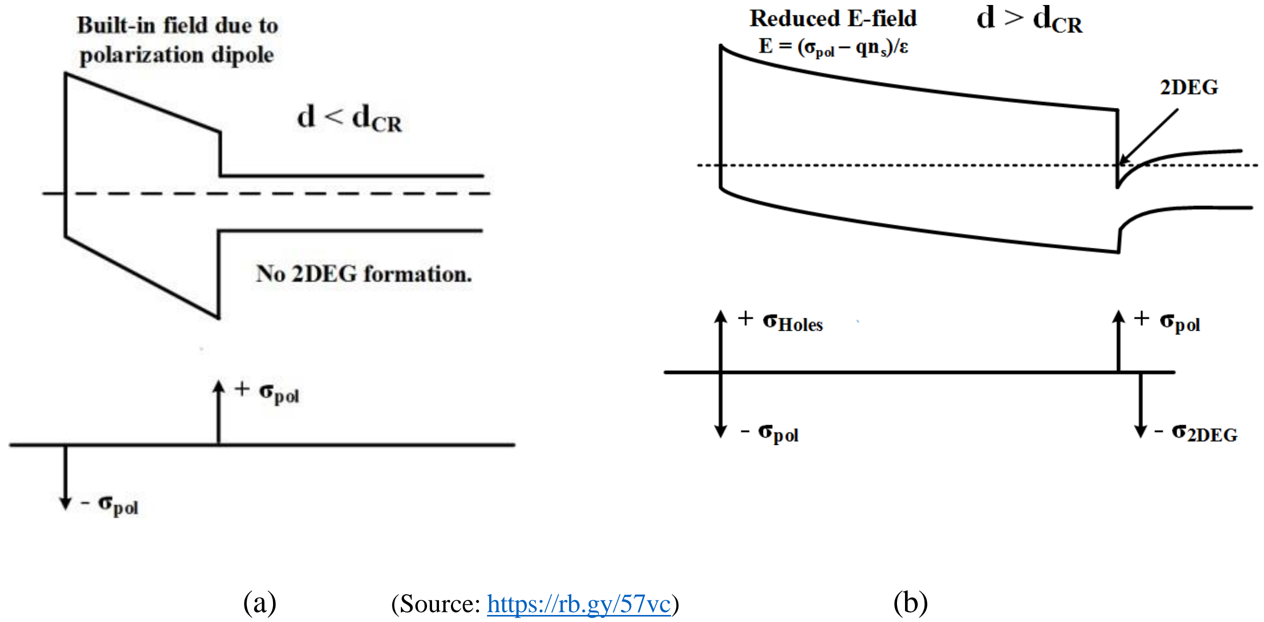
Fig. 2.1. (a) Energy band diagrams of AlGaN/GaN HEMT demonstrating band gap discontinuities (a) before creating the hetero-junction (b) band bending owing to hetero-junction formation (c) 2DEG density at the hetero-junction interface.

A High Electron Mobility Transistor (HEMT) is one heterostructure device made up of two different layers, the wide band gap semiconductor growing atop the tiny band gap material. Figure 2.1(a) displays the band structure diagram of a HEMT device before the design of the heterogeneous junction. Whenever the broad band gap material contacts with narrow band gaps material, what happens is a hetero-junction surface with requisite band bending to build a 2DEG is created (Fig. 2.1 (b)). Charged particles from donors impurity in the wide band gap compound (AlGaN) spread all across hetero-junction surface and are limited owing to the potential barrier formed by that of the hetero-junction interface. The electrons transfers occur owing to changes in such materials' the electron affinities (Ψ_s), the band gaps (E_g), & work functions ($q\varphi_s$). This electrons transfer process is continued till a Fermi level is attained among two different materials and also equilibrium state is achieved. Figure 2.1(c) displays a quantum potential well created just at hetero-junction interface, that is narrow enough to admit free electrons.

2.2 INTERFACE CHARGE

A conventional AlGaN HEMT devices with a flawless surfaces, i.e., no flaws or surface states formed during crystal growth and owing to the polarisation inversion found inside the AlGaN & GaN materials. Since the crystal created is in equilibrium, an uniform Fermi level may well be assumed over the AlGaN region. The existence of the same intensity polarisation charge (Fig. 2.2 (a)) is inadequate to generate the 2DEG just at AlGaN/GaN interface. A valence bandgap of AlGaN barrier reaches the Fermi level there at surface as when the thickness of AlGaN region (d) grows (Fig. 2.2 (b)). This increases electron transit across valence band of AlGaN barrier towards the conduction band for GaN, producing in the increased concentration of hole at the surfaces.

As a consequence, just at surfaces, a positively sheet charge is created, while at the AlGaN/GaN contact, an equivalent negatively sheet charge (2D Electron Gas) is generated. It is vital to remember that no 2DEG is formed till the surface holes gas is created. Additionally, increasing width of the AlGaN area has a large impact on the formation of surfaces hole gas. The critical thicknesses is just the least AlGaN thickness necessary to create the surfaces holes gas or 2DEG (dCR). Additionally, the critical thicknesses value is determined by bandgap of a AlGaN material in addition to the quantity of the polarization dipole produced in the crystalline structure.



(a) (Source: https://rb.gy/57vc) (b)

Fig. 2.2. 2DEG Formation for the situation of a perfect surface: (a) Zero 2DEG ($d < d_{CR}$) (b) 2DEG is produced at the AlGaN/GaN contact ($d > d_{CR}$).

Fixed charge density now at dielectric/ AlGaN contact n_{fix} may be written as

$$n_{fix} = n_{2D} + \Delta\sigma_{SP,diff} - \frac{Q_g}{q} \tag{2.1}$$

where, n_{2D} is the 2DEG charge density.

$\Delta\sigma_{sp}$ is total spontaneous polarization charges at AlGaN/GaN contact.

$\Delta\sigma_{SP,diff}$ is difference in net spontaneous polarization charges between the GaN and AlGaN layers

Q_g is charge inside the metal gate.

2.3 VI CHARACTERISTICS

The V-I Characteristics offers us the relationship among Drain Current (I_{ds}) and Drain Voltage (Vds) at fixed Gate Voltage (V_{gs}) . HEMTs function largely in depletion region, which implies that current that flows through all the devices regardless of whether the gate triggering voltage is supplied. The pinch-off voltage V_p is indeed potential that must be applied to the metal gate to cease current flow. The best technique to grasp the electrical behavior of HEMTs is to construct a mathematical framework and model the I-V characteristics.

Figure 2.3 displays the resultant Current-Voltage characteristics for varied gate voltage V_{GS} varying from 4 V to 0 V, with -4 V indicating the pinch off voltage V_p. Additionally, we may determine the ON resistance (R_{ON}) by calculating the curve's slope in the active zone. The less the R_{ON}, the better the device because then the power dissipation at input is low.

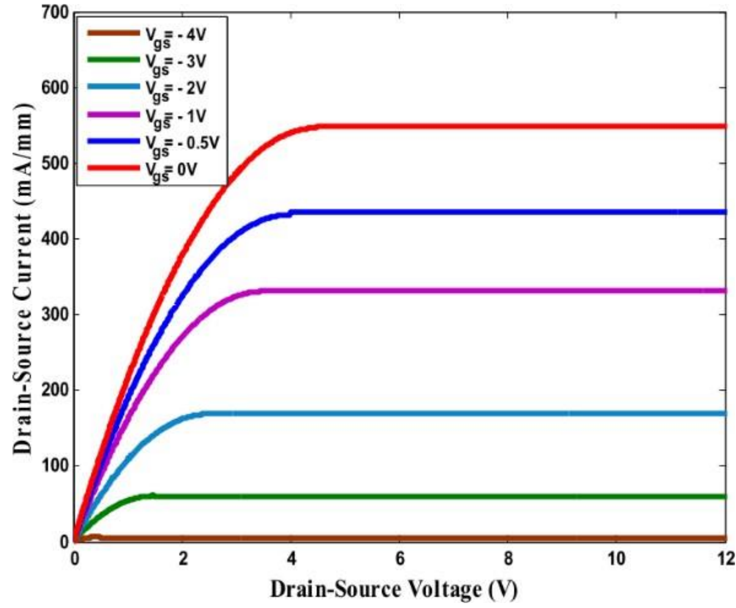


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Fig. 2.3. VI characteristics of a basic HEMT structure.

The VI Characteristics are modelled by the equation:

At triode region:

$$I_D = \frac{KP}{1+\theta(V_{GS}-V_{to})}\frac{W}{L}(V_{GS}-V_{to})(V_{DS}-R_S I_D-R_D I_D)-\left[1+\frac{\gamma}{2\sqrt{\varphi}}\right] \cdot \frac{(V_{DS}-RsI_D-RdI_D)^2}{2} \quad (2.2)$$

At saturation region:

$$I_D = \frac{KP}{1+\theta(V_{GS}-V_{to})}\frac{W}{L}\left[\frac{2\sqrt{\varphi}}{2(2\sqrt{\varphi}+\gamma)}\right] \cdot (V_{GS}-V_{to})^2 \quad (2.3)$$

where, KP - transconductance parameter.

V_{to} - threshold voltage.

L - the channel length

W - the channel width

R_d - the drain resistance.

R_s - the source resistance.

γ - body effect parameter

ϕ – surface potential

θ – mobility modulation constant

[36]Also, the ON resistance R_{ON} is calculated from the VI graph by using the formula:

$$R_{ON} = \frac{V_{DS}}{I_{DS}} \quad (2.4)$$

2.4 TRANSFER CHARACTERISTICS

Transfer Characteristics provides the proportion of the output Drain Current (I_{ds}) of the device to the input Gate Voltage (V_{gs}) along with the Drain Voltage (V_{ds}) remaining constant. It shows effect of the Gate Voltage on the device. Here also higher the saturation currents the better is the device.

2.5 TRANSCONDUCTANCE

Transconductance of a device is its electrical characteristic that relates the current that flows throughout a device's output terminal to the potential across its input terminal. It is produced by running an AC simulation. A greater transconductance suggests that the device may be utilized to provide stronger gain with all the parameters being unchanged and better switching frequency. So a device with better transconductance is always preferred.

The transconductance is computed by calculating the change in the rate of drain current (I_{ds}) in proportion to Gate-Source voltage (V_{gs}) whilst maintaining its Drain-Source voltage (V_{ds}) fixed.

The formula is given by:

$$g_m = \frac{\partial I_d}{\partial V_{gd}} |_{V_{ds}} \tag{2.5}$$

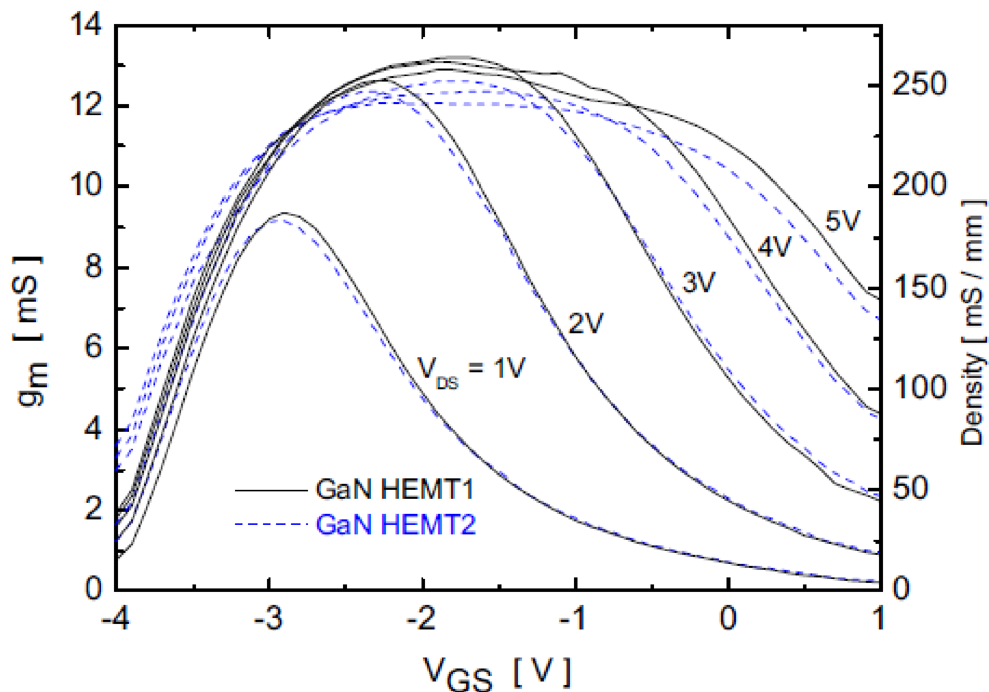

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Fig. 2.4. Transconductance of two basic GaN HEMTs

2.6 DRAIN LEAKAGE CURRENT

The Drain Leakage Current is its output current of Drain calculated by altering the Gate Voltage while the devices is in an off state. This is a very important metric as less leakage current means less power dissipation when the device is not being used, hence improving the overall battery life of the device. Also, we can calculate the I_{ON} to I_{OFF} ratio which can be used to know whether the device can be used at higher frequencies or not. A higher value of this ratio is preferred.

2.7 GATE CAPACITANCES

The gate capacitance values that are most critical to examine include Gate - Source Capacitance (C_{GS}) & Gate - Drain Capacitances (C_{GD}). This capacitances serve as indicators to evaluate if the devices will have a larger or reduced switching delay. The less these capacitances, lesser will be the switching delay. The sample plots for Gate Capacitances are shown in figure 2.5.

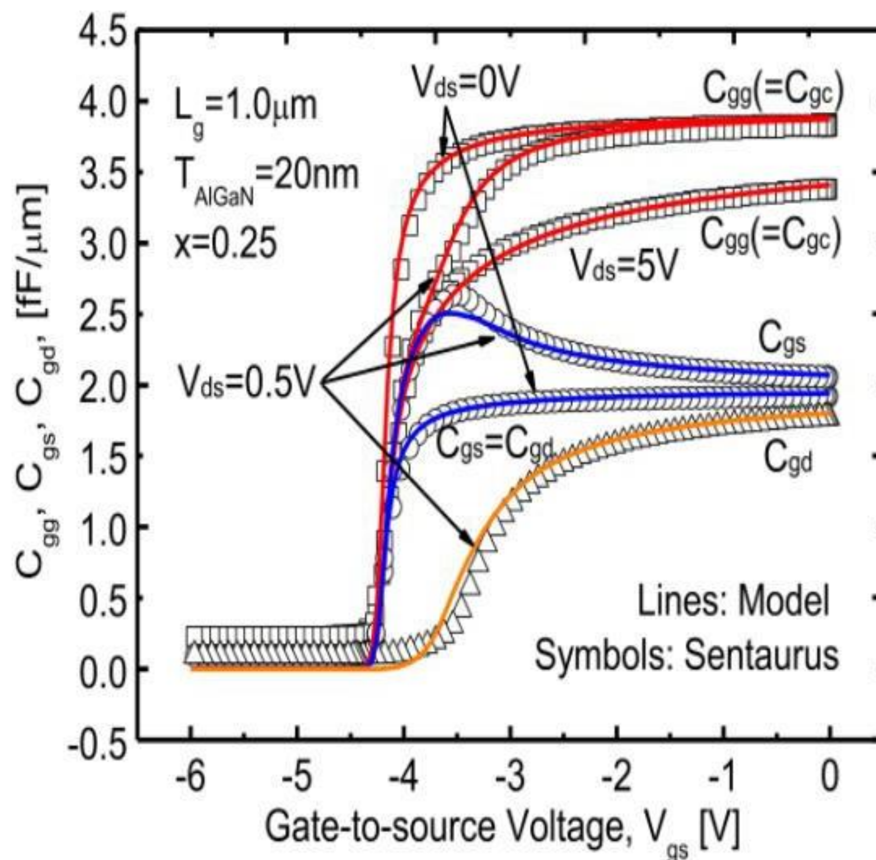

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Fig. 2.5. Gate Capacitances plotted against V_{GS}.

2.8 BREAKDOWN VOLTAGE

The breakdown voltage is a very important parameter to study. For calculating the breakdown voltage, we first deplete the entire channel by applying a negative Gate Voltage and then start increasing the drain voltage. At some voltage the device will have an Avalanche breakdown and the current spikes. This voltage is the breakdown voltage. A larger breakdown voltage indicates that the device may be used for higher drain voltages, which is ideal for power devices because the voltages in Electric Vehicles are extremely high.

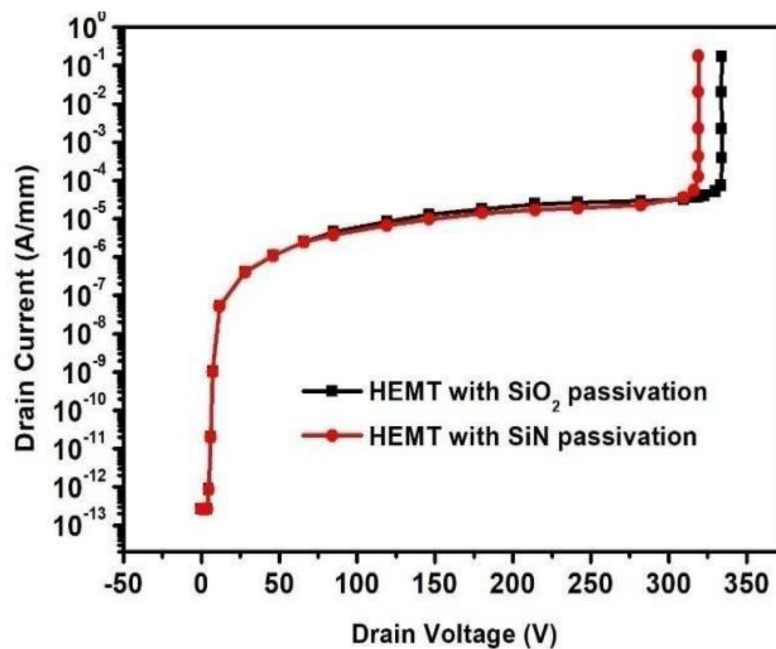

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Fig. 2.6. Breakdown Voltage of conventional GaN with different passivation

2.9 GATE SWITCHING DELAY

Gate switching delay of a device is its time it requires for such a device to turn ON from an OFF state. It is calculated using the following formula:

$$\tau = R_{ON}.C_G \tag{2.6}$$

where,

$$R_{ON} = V_{DS}/I_{DS} \tag{2.7}$$

$$C_G = C_{GS} + C_{GD} \tag{2.8}$$

CHAPTER 3
REASERCH PROGRESS IN GaN-BASED HEMT

The GaN-based HEMTs performance is detailed in this chapter with this literature survey. This chapter briefs the following, the overall status of research on the device and the structure dependency on the device parameters like drain current and on-resistance etc. And furthermore, it presents the important device design criteria for the measurements such the gate length L_g as well as the barrier thickness.

3.1 LITERATURE SURVEY

To identify the key factors to improve the E-MODE GaN HEMTs for output performance a detailed literature research was conducted.

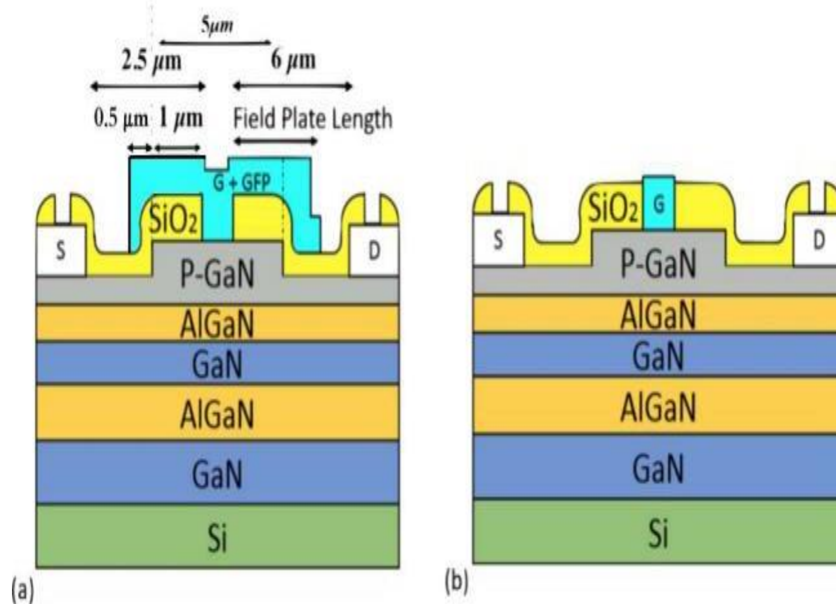


Fig. 3.1. Device construction of (a) FP-HEMT as well as a (b) typical conventional HEMT. [37]

Chun-Hsun Lee et al. constructed gate field plate using p-GaN/AlGaN/GaN/AlGaN double heterostructures. The Voltage-Current transfer curves confirmed the existence of such a subthreshold zone.

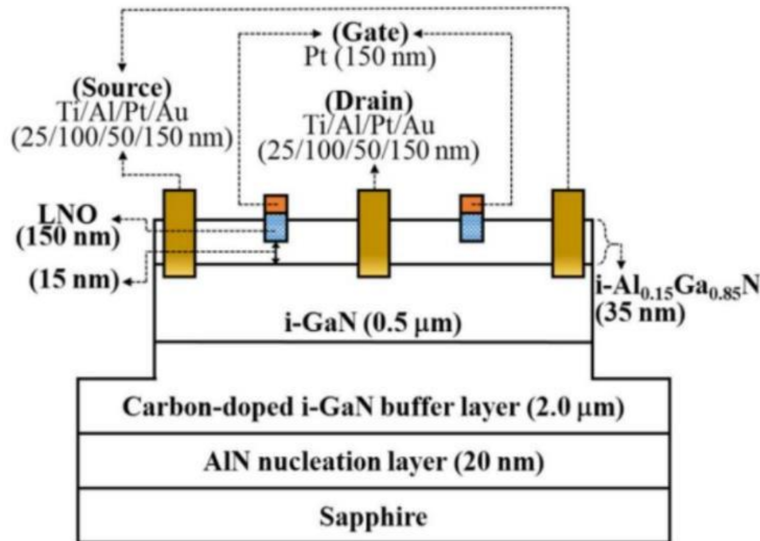


Fig. 3.2. Schematic arrangement of AlGaN/GaN E-MOSHEMTs.[38]

In this research, the gate-recessed design as well as the LiNbO3 ferroelectric material were utilized. Utilizing a pulsed laser deposit approach, the gate insulators LiNbO3 ferroelectric films have been applied over the photoelectrochemically cut gate-recessed portions of AlGaN/GaN E-MOSHEMTs.

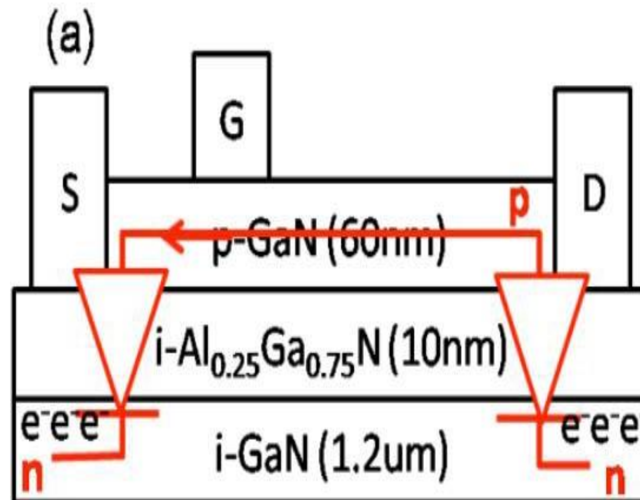


Fig. 3.3. (a) Schematic representation of the device before detaching the p-GaN capping layer just above channel. Its built-in p-i-n diodes were also displayed.[39]

Liang-Yu Su et al. established parallel conduction routes of a p-GaN layer with 2-D electrons gas (2DEG) channels within this HEMT structure and exhibited a voltage level (Vth) of 4.3 V by altering its built-in potential of the diode created between both the p-GaN & channels by alloy temperature.

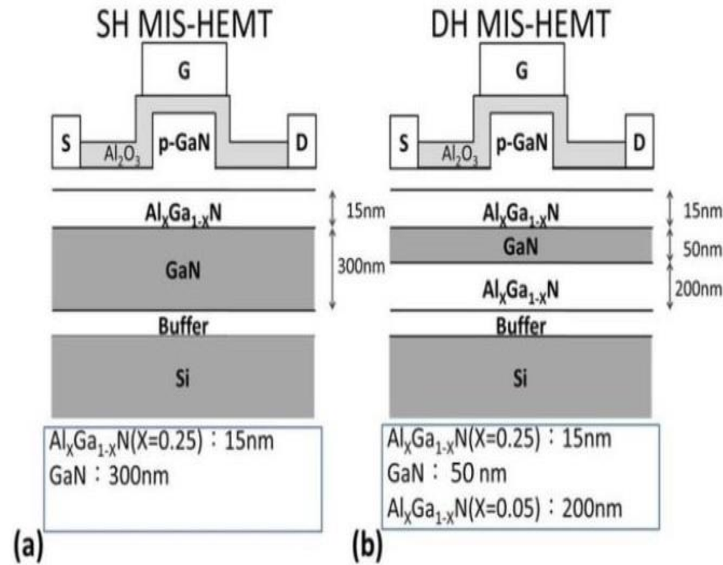


Fig. 3.4. Device architectures of (a) SH MIS-HEMT and (b) DH MIS-HEMT.[40].

h

An enhanced mode (E-mode) AlGaN/GaN/AlGaN multilayer (double) heterostructure was suggested in this work. The current collapse phenomena was examined utilizing E-mode MIS & Schottky gate HEMTs. The findings reveal that current collapse is prevented in devices possessing a double heterostructure.

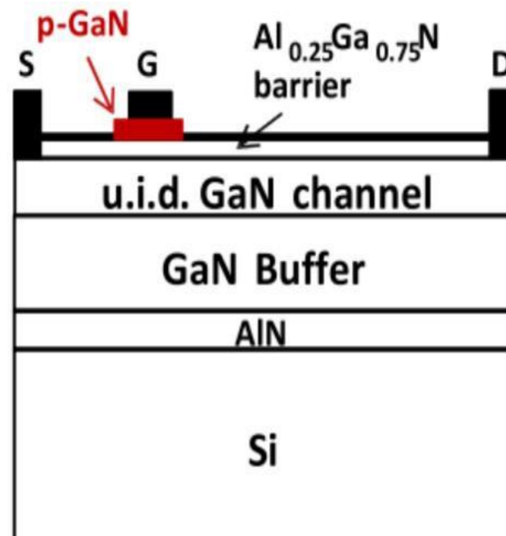


Fig. 3.5 Schematic cross - sectional view of the gadget under test. Reported transistors are Enhancement mode AlGaN/GaN HEMTs having the p-type gate. [41].

Isabella Rossetto et al. gives an experimental proof for time-dependent breakdown of GaN-on-Si power high-electron-mobility transistors using p-GaN gates under forward gate stress.

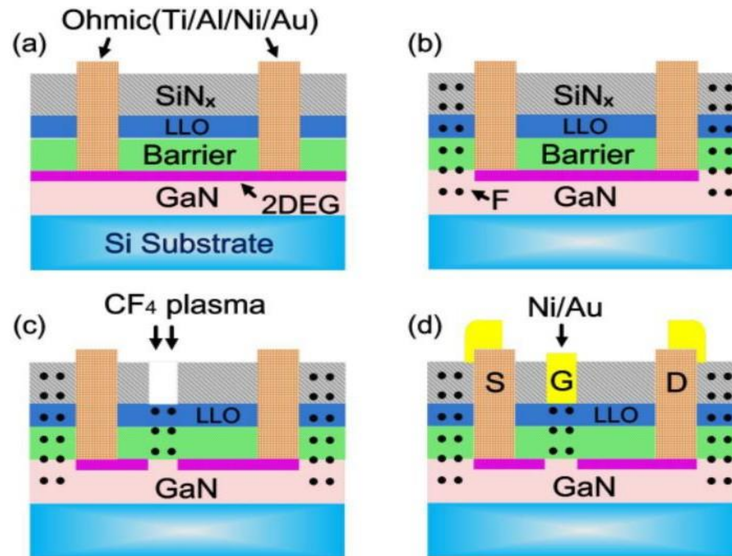


Fig. 3.6. Planar construction of E-mode LLO-AlGaN/ GaN MIS-HEMTs is depicted. (a) The creation of an ohmic contact. (b) Isolation of planar devices. (c) Implantation of CF4 plasma ions in the gate region. (d) Interconnections and gate metallization. [42]

Shu Yang et al. explore enhancement-mode (E-mode) (E-mode) LaLuO3 (LLO)-AlGaN/GaN metal-insulator-semiconductor high-electron mobility transistors (MIS-HEMTs) created employing fluorine (F) plasma ion implantation in a gate-dielectric-first planar approach.

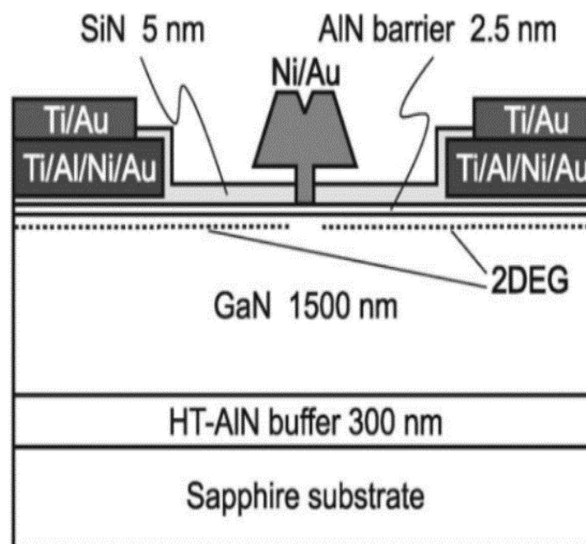


Fig. 3.7. Schematic cross - sectional view of Enhancement -mode AlN/GaN HFETs.[43]

Mode of high-performance augmentation (E-mode). A new technique for constructing AlN (2.5 nm)/GaN heterostructure field-effect transistors (HFETs) leveraging SiN passivation by catalytic chemical vapor deposition was devised. (Cat-CVD). Masataka Higashiwaki et al.

showed that the inclusion of Cat-CVD SiN just on barrier layer may impact the generation of 2-D electron gas (2DEG) inside an AlN/GaN heterostructure

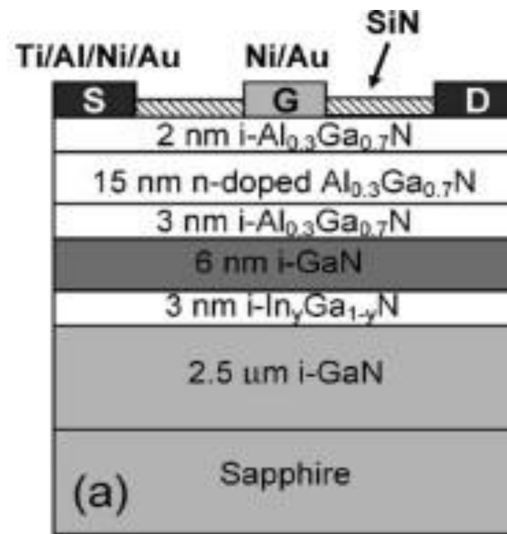


FIg. 3.8 (a) InGaN-notch DH-HEMT cross - sectional view. An 3-nm-thick $In_yGa_{1-y}N$ material (y = 5% & 10%) is injected into the channel area, retaining existing 6-nm-thick GaN region as that of the channel layer. [44]

The comprehensive dc and radio-frequency features of the $Al_{0.3}Ga_{0.7}N/GaN/In_{0.1}Ga_{0.9}N/GaN$ double-heterojunction HEMT (DH-HEMT) architecture are provided by Jie Liu et al. .This structure incorporates a small (3 nm) In0.1Ga0.9N notched layer implanted 6-nm away from the AlGaN/GaN heterojunction interface.

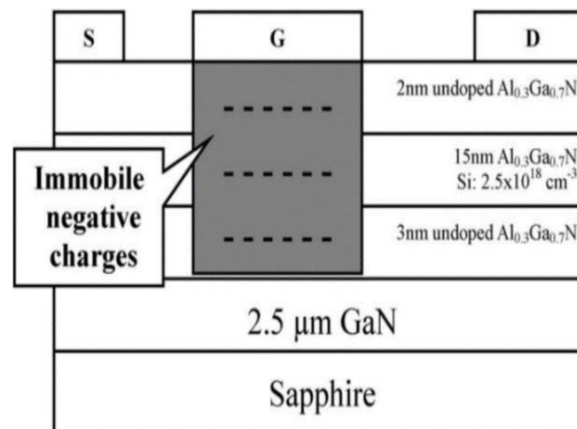


Fig. 3.9 AlGaN/GaN HEMT having directly incorporated immobile negative charges behind the gate.[45]

Yong Cai et al. presents a technique for accurately adjusting overall threshold voltages (V_{th}) for AlGaN/GaN HEMTs using fluoride-based plasma treatment process.

The V_{th} of AlGaN/GaN HEMTs may be continually modified using this approach from 4 V in a conventional Depletion-mode (D-mode) AlGaN/GaN HEMT down to 0.9 V in an E-mode AlGaN/GaN HEMT.

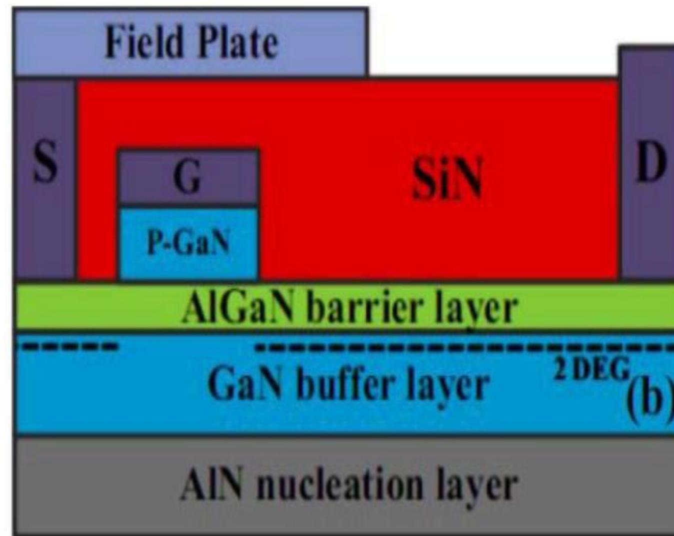


Fig. 3.10 The manufacturing of the p-type GaN HEMT with L_{GD} = 7m & Source field plate length L_{FP} = 10m is represented graphically. [46]

A new step has been carved Simulating a GaN buffer architecture in combination with such a narrow GaN buffer is examined. The breakdown voltage may be enhanced by employing the both thin GaN buffers and the step-etched GaN architecture. The narrow GaN buffer may lower conductivity while also decreasing the upward electric field.

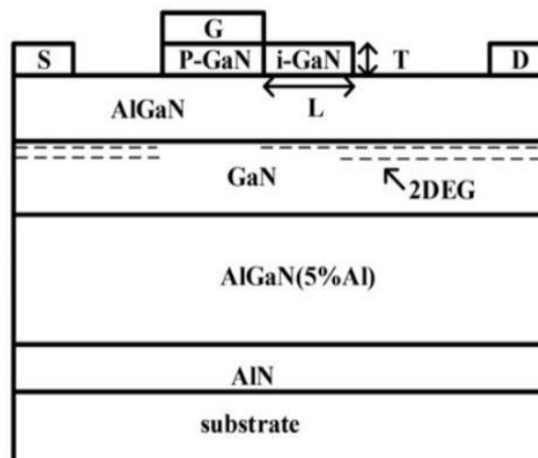


Fig. 3.11 The revolutionary E-mode AlGaN/GaN HEMTs with such a p-type GaN gate can be seen in cross-sectional view.[47]

The drift-diffusion model, which contains fundamental Poisson, drift-diffusion, & current-continuity equations, was applied in the simulation. As compared to standard E-mode AlGaN/GaN HEMTs, the breakdown voltage level may be enhanced by 192.2%.

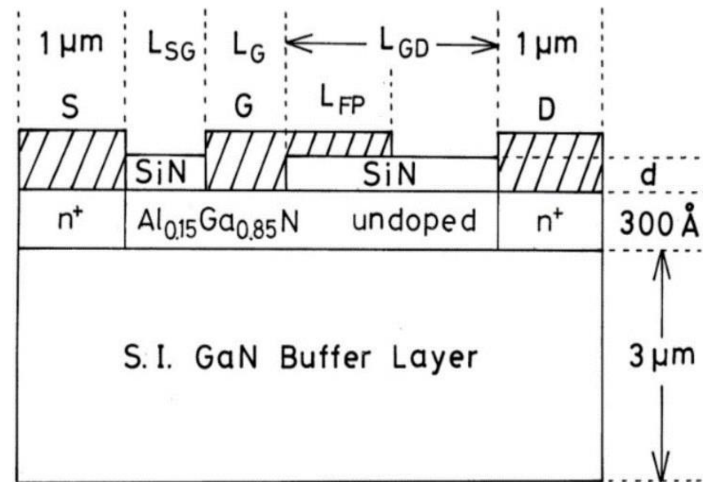


Fig. 3.12. This study looked at the device structure. [48]

The off-state breakdown properties for field-plate AlGaN/GaN HEMTs were explored in two dimensions. The gate-to-drain separation is 1.5 μm, as well as the parameters are just the width of the SiN oxide layer d as well as field-plate length L_{FP}. With a modest 'd' of 0.1μm, breakdown potential value (V_{br}) rises with L_{FP}, reaching its highest level (~400 V) at LFP = 0.3 μm and falling as L_{FP} lengthens.

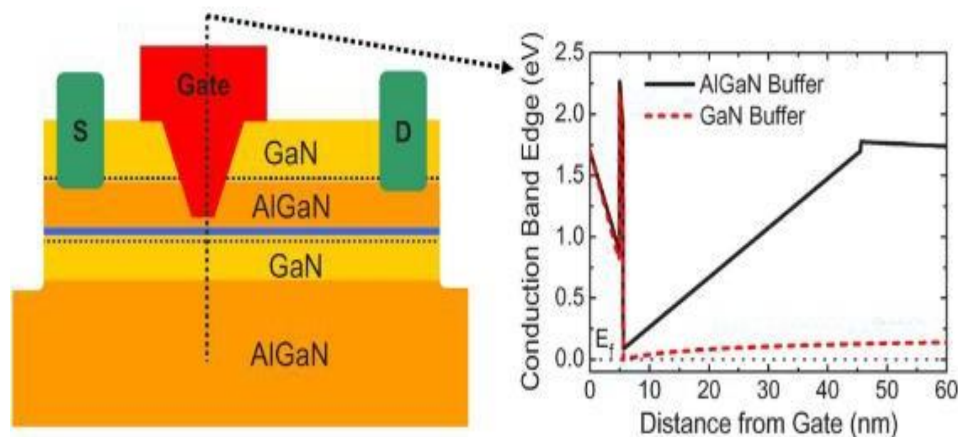


Fig. 3.13 Cross-sectional schematics of buffer-engineered V-gate GaN HEMT. The gate region's band structure is illustrated in contrast to a standard GaN buffer HEMT [49].

Rongming Chu et al. suggest and implement V-gate GaN HEMTs with tailored buffer for normally-off operation. Net negative polarization charges are created beneath a GaN channel via incorporating an AlGaN buffer. True typically off functioning with decreased dc-

RF dispersion was attained employing the engineered-buffer structure in combination with the deep-recess V-gate structure.

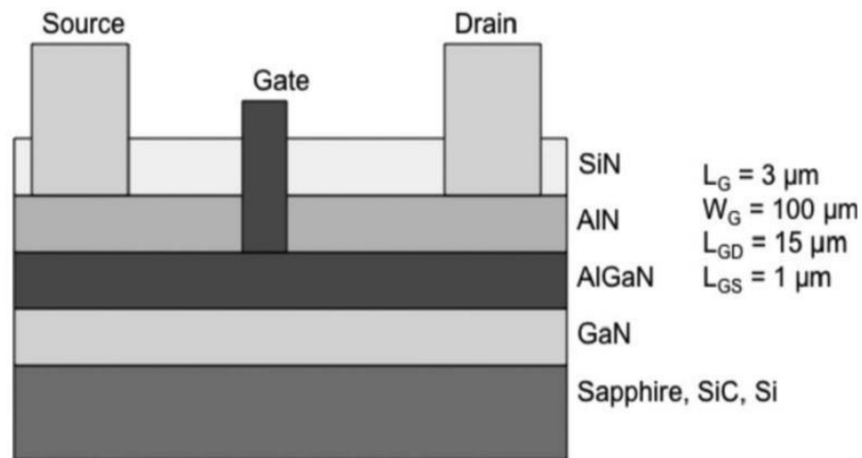


Fig. 3.14 AlN/ultrathin AlGaN/GaN HEMT cross-sectional diagram.[50]

To reliably control voltage level through AlGaN/GaN high-electron-mobility transistors, an innovative device structure trying to incorporate an extremely thin AlGaN protective barrier surmounted by such an AlN layer inside the source-drain access region was incorporated, and a repetitive threshold voltage of +0.21 V of 4-nm AlGaN barrier layer was demonstrated.

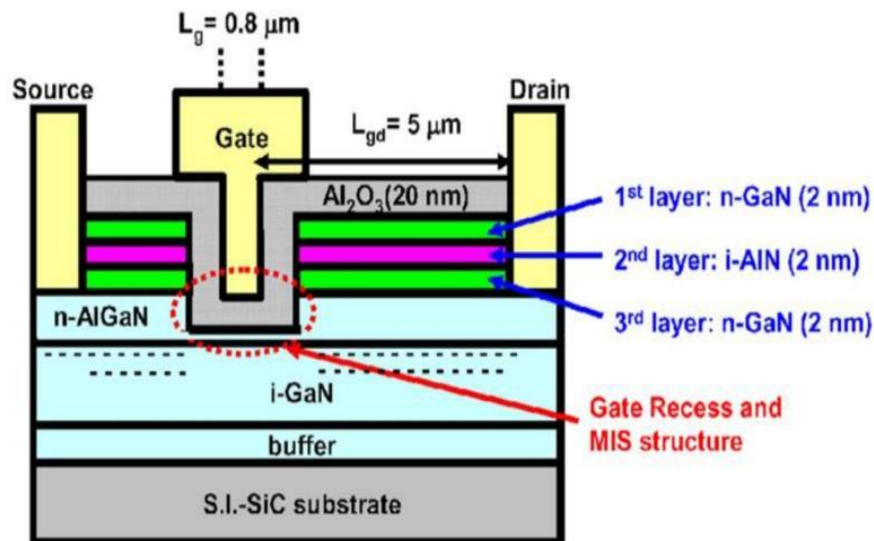


Fig. 3.15 AlGaN/GaN MIS-HEMT having a triple cap layers, recessed gate structure, & high-k dielectrics is illustrated in a graphical cross-sectional view. [51]

Specifications of high-performance E-mode GaN MIS high-electron mobility transistor (MISHEMT) structures have been given by Masahito Kanamura et al. .High drain current and full enhancement-mode functioning are achieved in systems with either n-GaN/i-AlN/n-GaN triple cap layers, recessed-gate structure, & high-k gate dielectrics. Highest drain current & thresholds voltage (V_{th}) is 800 mA/mm & +3 V, correspondingly.

Table 3.1 State of the art of GaN HEMTs

S. No.	Ref. paper	Lg (μm)	Lgd (μm)	Lgs (μm)	Gm (mS)	Im(mA /mm)	Vbr (v)	Ron (Ω.mm)	Wg (gate width) (μm)
1	[1] Alex Man Ho Kwan *et al.* (2012)	1.5	2	2	167	310	419	1.50	5
2	[7] Bin Lu *et al.* (2010)	0.95±0.1	5	….	130	450	643	4.3	....
3	[11] Chun-Hsun Lee *et al.* (2018)	3	6	2.5	10	110	….	….	50
4	[12] Cheng Liu *et al.* (2015)	1.5	15	...	112	730	703	....	....
5	[13] Ching-Ting Lee *et al.* (2015)	1	….	….	115.3	500	…..	….	50
6	[14] Chao Chen *et al.* (2011)	3	....	....	154.6	547	20	....	120
7	[18] Finella Lee *et al.* (2015)	4	6	2	....	220	....	....	50
8	[20] Guohao Yu *et al.* (2012)	12	12	5	....	35	....	115	100
9	[21] Huaxing Jiang *et al.* (2018)	1.5	3	3	130	550	....	9.2	10
10	[22] Haijun Guo *et al.* (2017)	1.4	6	1	….	430	....	….	....
11	[24] Isabella Rossetto *et al.* (2016)	1.3	15	1	….	350	….	…..	0.25
12	[25] Takuma Iwamoto *et al.* (2021)	0.3	1.5	0.5	....	500	400	....	....

13	[26] Jie Liu *et al.*(2007)	1	1	1	150	210	....	....	10
14	[27] Jiejie Zhu *et al.* (2017)	1 to 9	3	3	91	330	....	11	100
15	[32] Chih-Hao Wang *et al.* (2015)	3	6	2	....	150	....	....	50
16	[33] Ling Yang *et al.* (2018)	0.2	2.2	1.6	412	845	183	....	2×50
17	[34] Liang-Yu Su *et al.* (2014)	4	16	2	….	60	1630	....	50
18	[36] Masataka Higashiwaki *et al.*(2007)	100-180	….	….	400	800	....	....	100
19	[37] Masahito Kanamura *et al.* (2009)	0.8	5	..	155	800	90	6.2	40
20	[40] N. Ketteniss *et al.* (2012)	1	....	....	250	500	....	....	
21	[48] Raphael Brown *et al.* (2014)	6	....	....	140	400	9Mv	....	100
22	[49] Rongming Chu *et al.* (2008)	0.9	1	0.5	....	250	90	....	2 × 75
23	[50] Sen Huang *et al.* (2015)	1	3	2	....	450	....	....	100
24	[51] Shuxun Lin *et al.* (2016)	2	3	1.5	....	630	....	4.85	....
25	[52] Shenghou Liu *et al.* (2011)	2	....	....	120	90	....	....	80
26	[56] Shin-Yi Ho *et al.* (2017)	3	6	2	26	60	….	1.2	50
27	[57] Shu Yang *et al.* (2013)	2	5	….	180	350	450	1.03	….
28	[58] Ting-Hsiang Hung *et al.* (2013)	2	….	....	43	140	....	20	....

30	[59] Travis J. *et al.* (2009)	3	15	1	33	25	....	....	100
29	[60] Tian-Li Wu *et al.* (2015)	0.7	0.75	0.75	....	90	....	....	10
31	[61] Uttam Singisetti *et al.* (2010)	0.18	....	0.77	225	740	15	2.0	....
32	[63] Ronghua Wang *et al.* (2011)	8	....	....	420	600	~29	....	50
33	[66] Hao Wu *et al.* (2021)	1.5	1-7	1.5	....	225	900	2.6	....
34	[69] Yueh Chin Lin *et al.* (2017)	2	15	3	165	648	....	9.4	....
35	[71] Z. H. Feng *et al.* (2010)	0.35	....	1.5	280	850	....	....	....
36	[70] Yong Cai *et al.* (2006)	1	2	1	0.15	450	….	….	....
37	[72] Zhe Xu *et al.* (2013)	2	6	2	....	288	....	36.4	....

CHAPTER 4

A NORMALLY OFF GAN HFET WITH P-TYPE GAN GATE

In this chapter we discuss the very first device, that is a GaN HEMT with the p-GaN Gate with length 0.8µm. Once knowing about the device structure and composition we will check various parameters which are needed to know whether the proposed device is more efficient and reliable than already available devices in the market.

4.1 STRUCTURE

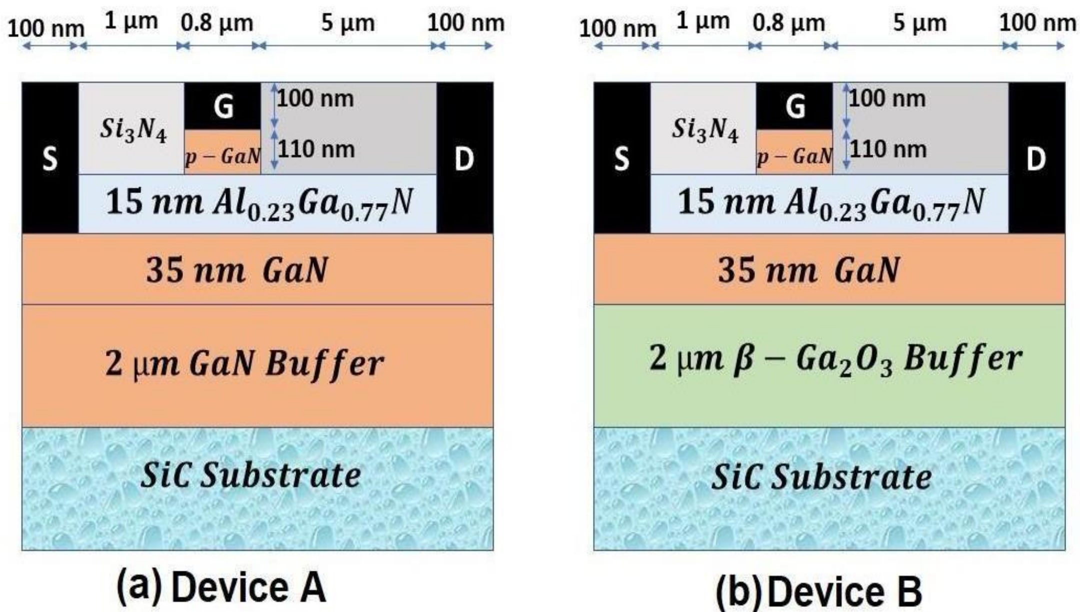


Fig. 4.1 Normally-off GaN HEMT with p-type GaN

The vertical cross section view of p-type GaN gate with GaN buffer and with a β-Ga_2O_3 buffer are seen in Fig 4.1.

The total length of the device stands at 7µm. The length of Source and Drain is 0.1µm or 100nm. The gate length is 0.8µm and the distance between Source and Gate is 1µm whereas the distance between Gate and Drain is 5µm. The gap between Source, Gate and Drain is filled with Silicon Nitride (Si_3N_4).

Silicon Carbide (SiC) is used as the substrate for our device followed by a 2µm length GaN Buffer. This is further followed by a thin layer (35nm) of GaN and then a thinner (15nm) layer of $Al_{0.23}Ga_{0.77}N$, i.e., it has 23% Aluminum Nitride (AlN) and 77% of Gallium Nitride (GaN).

4.2 RESULTS AND DISCUSSIONS

Below are the 10 key parameters that we considered checking the efficiency and reliability of the device we proposed.

4.2.1 Band Diagram

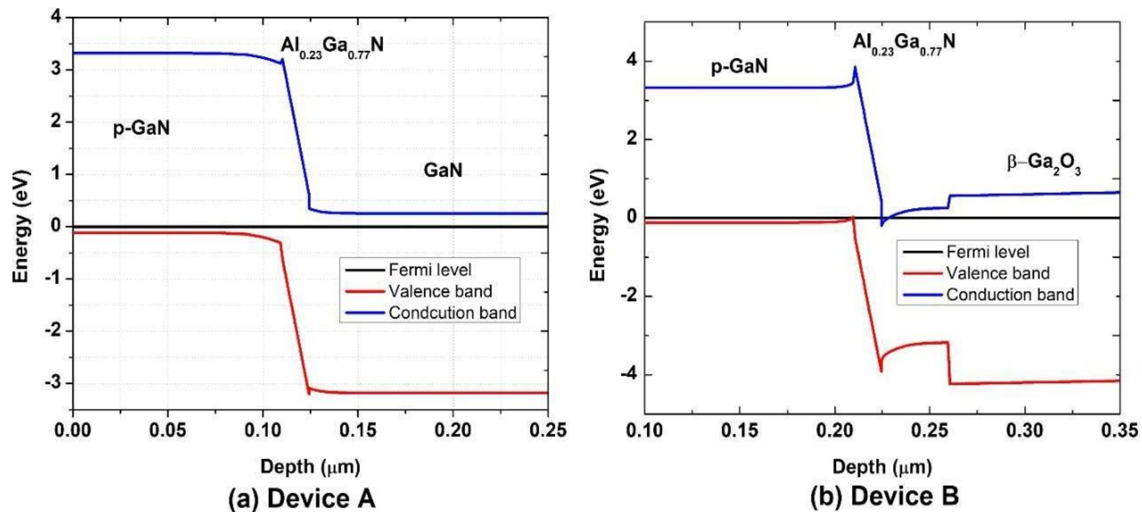


Fig. 4.2 Band Diagram of the proposed device

The Ban Diagram of the standard available device is compared against the proposed device. A clear 2DEG well is formed in the proposed device creating a well/barrier where electrons are confined. This ensures that there isn't any need for external polarization as there will be an internal polarization due to the high concentration of electrons in the well. We can also see that the difference between Valence Band and Conduction Band is higher in the proposed device which makes the device tolerate higher electric fields which ensures the proposed device be operated at higher breakdown voltages.

4.2.2 Interface Charge

The AlN/β-Ga2O3 heterostructure's interface charge details are shown in Figure 4.3. The suggested heterostructure has an interface charge density (n_s) of 8.0×10^{12} cm^2.
As shown in Eq. (4.1), the spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pz}) of various materials can be used to represent the polarization-induced sheet charge density (Δσ) at the heterojunction interface. The polarization constants of groups III-nitride and β-Ga2O3 are shown in Table 4.1.

$$\Delta\sigma = -\Delta P = P_{sp}^{(sub)} - [P_{sp}^{epi} + P_{pz}^{(epi)}] \tag{4.1}$$

The piezoelectric polarization can be represented as

$$P_{PZ}^{(epi)} = 2\left[e_{31}^{(epi)} - \frac{C_{13}^{(epi)}}{C_{33}^{(epi)}} e_{33}^{(epi)}\right] \times \frac{a^{(epi)}-a^{(sub)}}{a^{(epi)}} \quad (4.2)$$

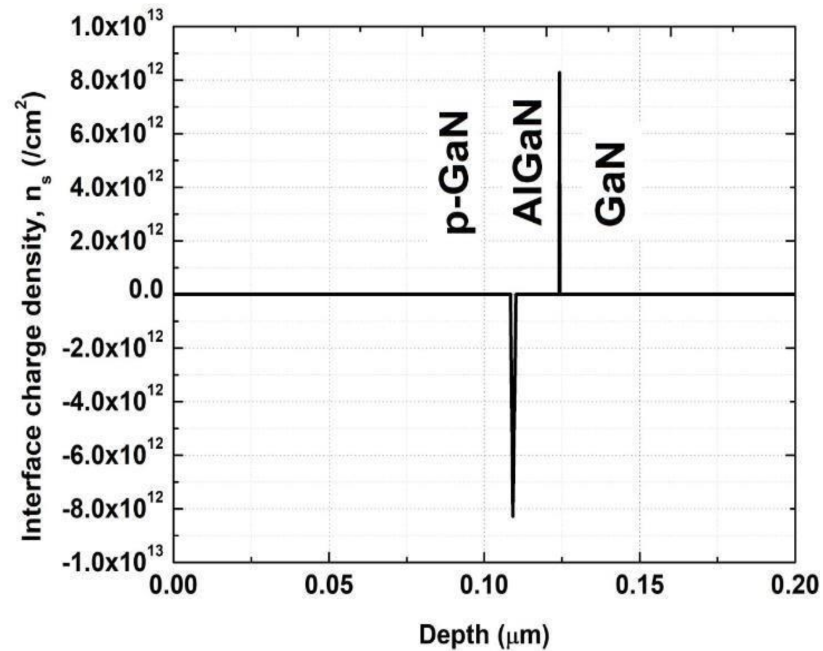


Fig. 4.3 Interface Charge

Table 4.1 Structural parameters and polarization constant of β-Ga2O3, as compared with group III-nitride binary elements.

Parameter	AlN	GaN	InN	β-Ga_2O_3
Lattice Constant a (A°)	3.113	3.182	3.541	a=12.23 b=3.04 c=5.80
Piezoelectric constant SP (C/m^2)	1.333	1.339	1.164	0
Piezoelectric constant e_{33} (C/m^2)	1.642	0.615	1.058	0
Piezoelectric constant e_{31} (C/m^2)	-0.669	-0.358	-0.549	0
Elastic Constant c_{33}	373	398	224	330
Elastic Constant c_{13}	108	106	92	125

4.2.3 Electron and Hole Concentration

Fig 4.4(a) and Fig 4.4(b) shows TCAD simulation of the Electron and Hole concentration of GaN buffer device for three different Drain-Source Voltage (V_{DS}) , which are +2V, +4V and +6V respectively.

Similarly, the TCAD simulation of Electron and Hole concentration for the proposed device with β-Ga_2O_3 buffer is seen in Fig 4.5(a) and Fig 4.5(b) for the same Drain to Source Voltages.

a. GaN Buffer

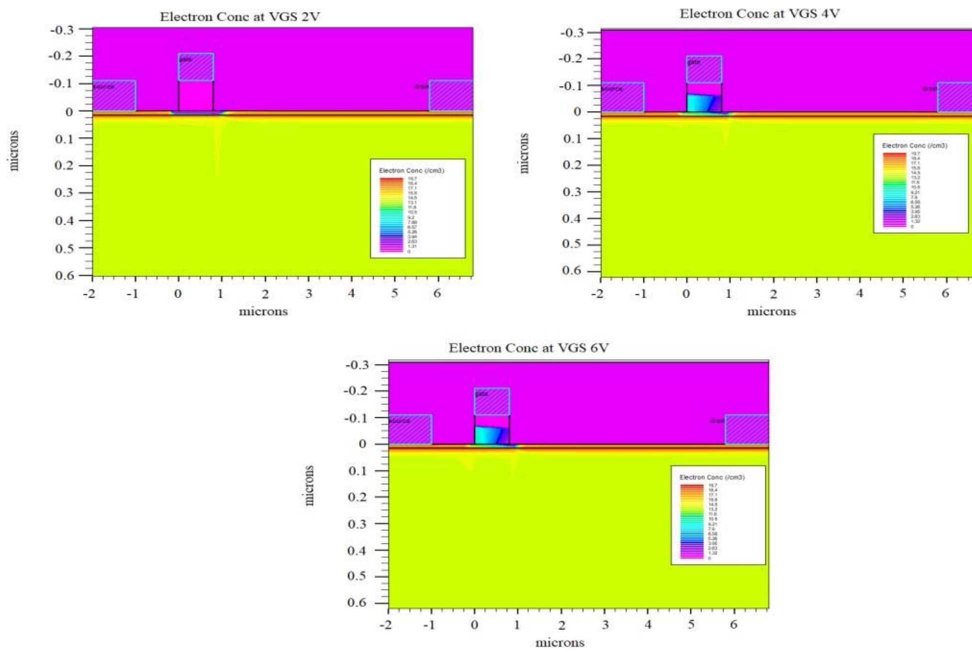


Fig. 4.4(a) Electron Concentration of different V_{DS} levels

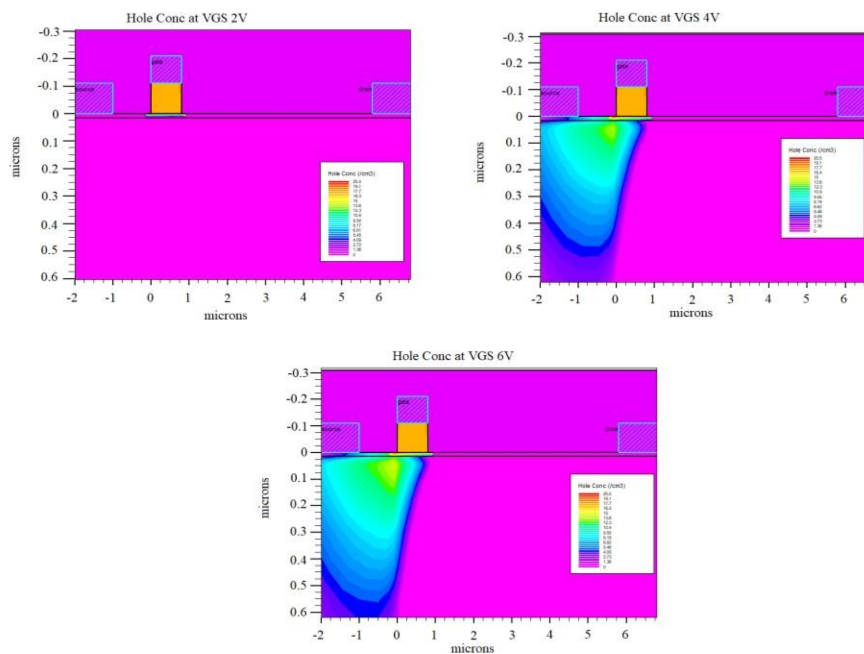


Fig. 4.4(b) Hole Concentration of different V_{DS} levels

b. β-Ga_2O_3 Buffer

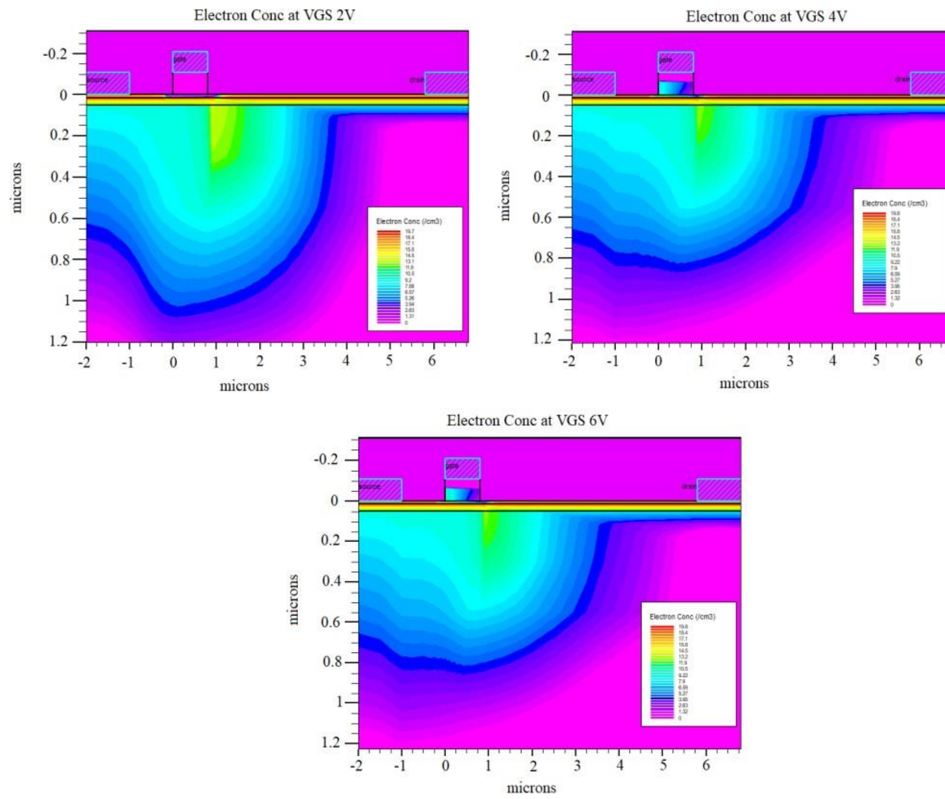


Fig. 4.5(a) Electron Concentration of different V_{DS} levels

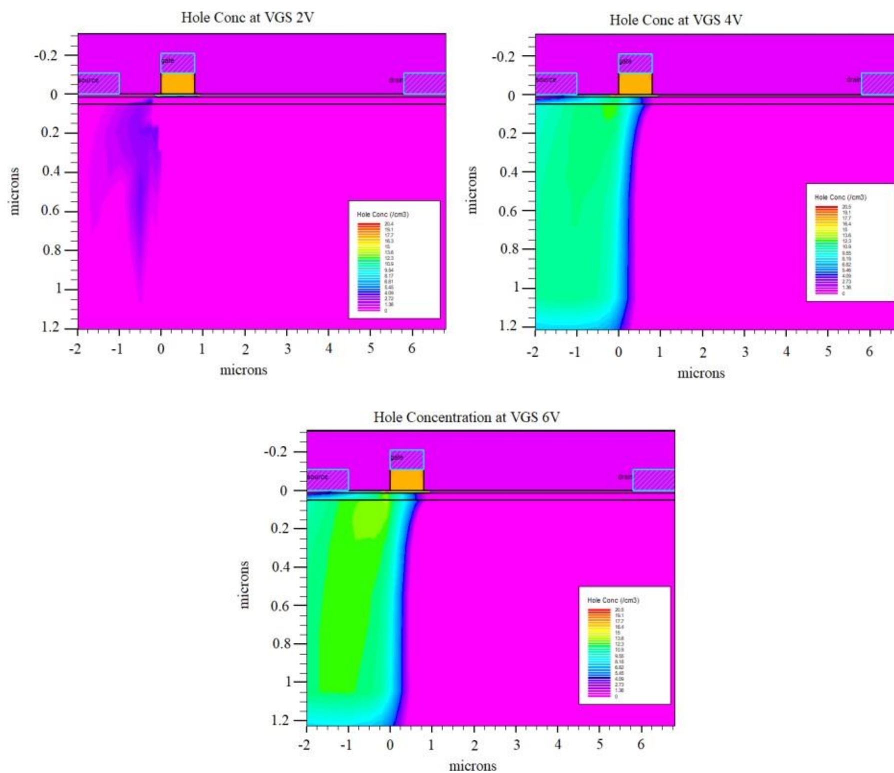


Fig. 4.5(b) Hole Concentration at different V_{DS} levels

4.2.4 V-I Characteristics

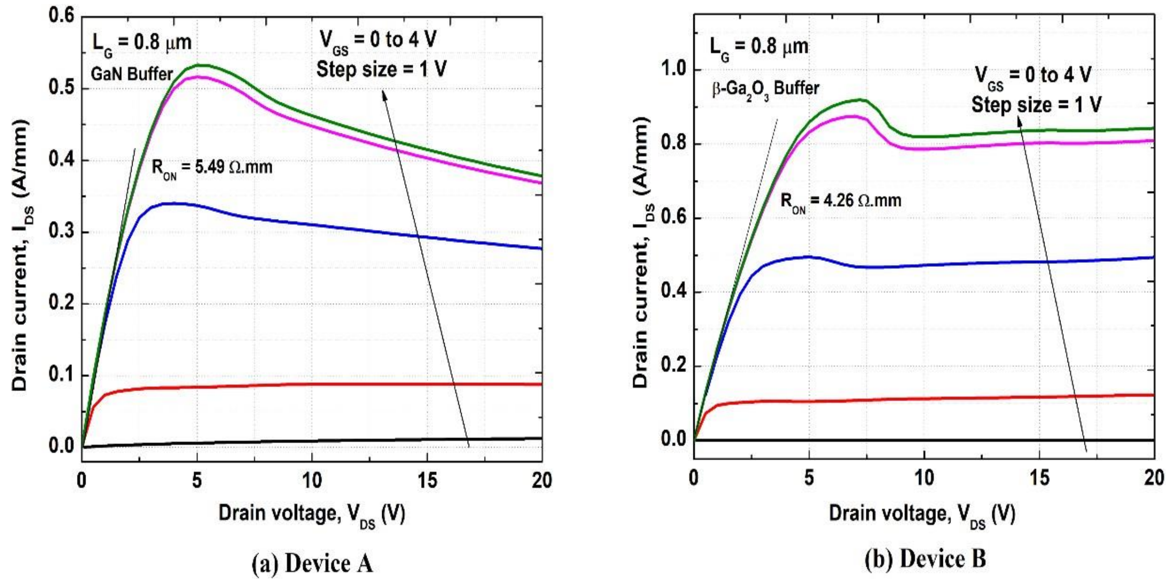


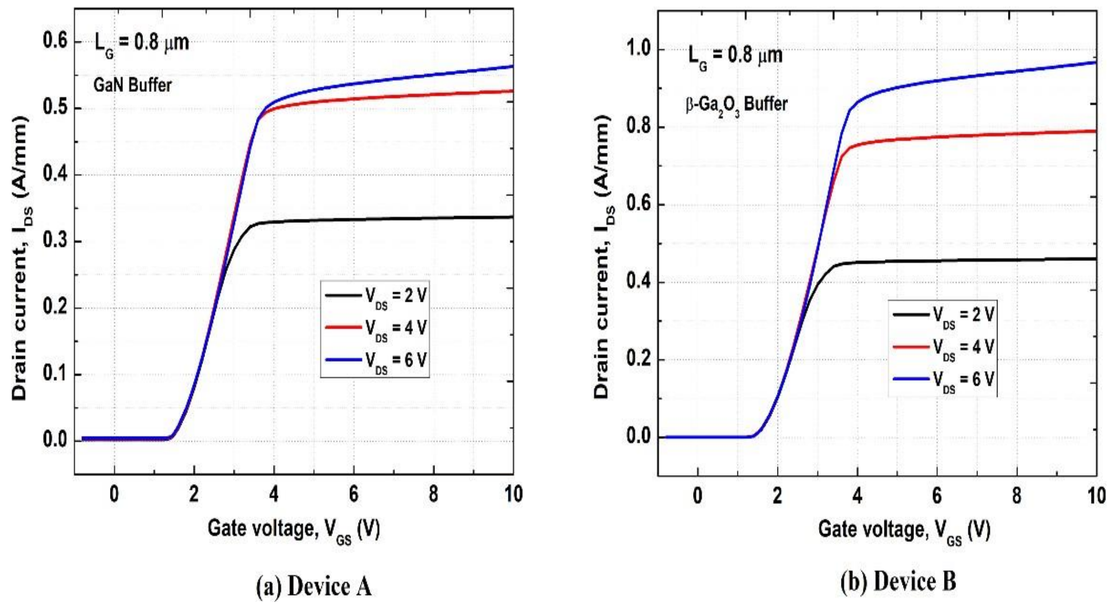
Fig. 4.6 V-I Characteristics

This figure shows the V-I characteristics of the existing device and the proposed device. The V-I characteristics are run for various Gate voltages varying from 0V to 4V with a step size of 1V. The drain voltage is swept from 0V to 20V. The respective drain currents for each gate voltage are plotted against the drain voltage for a device of gate length, L_g=0.8μm. The maximum current saturation is 0.53A/mm for the first device whereas it is 0.92A/mm in the case of the second device. We can see that the saturation currents of the second device are higher than the first device for same gate voltages which is due to the higher concentration of 2DEG because of the confined electrons in the well. This also means that the second device will deliver more output power comparatively due to higher output current for same voltages. Once the V-I Characteristics are plotted, the on resistance, R_{ON} is plotted by taking a slope of the V-I curve for a particular gate voltage where the current is maximum. On comparison it is seen that the first device has an R_{ON} = 5.49 Ω.mm while the proposed device has an R_{ON} = 4.26 Ω.mm. This allows the second device to have lesser power dissipation at the input for the same voltages. Hence this gives us the chance to operate at higher voltages.

4.2.5 Transfer Characteristics

The simulation results for transfer characteristics of the existing device and proposed device are shown in Fig. 4.7. The transfer characteristics show the effect on output (I_{DS}) for

varying input (V_{GS}).The drain voltages are varied from +2V to +6V and the gate voltage is swept from 0V to +10V and the respective drain current is plotted for each drain voltage.

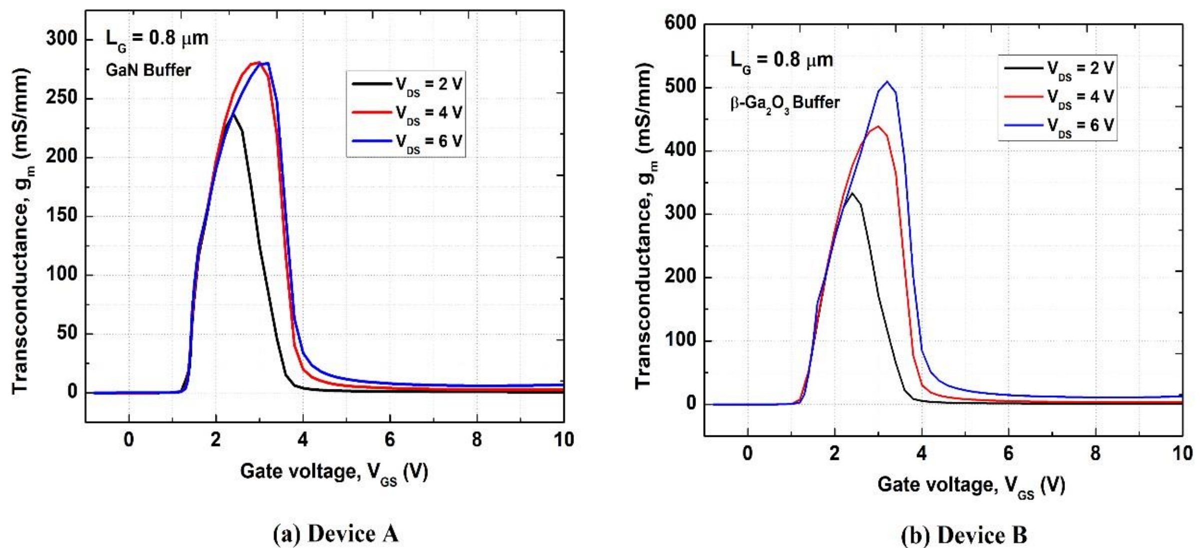


(a) Device A (b) Device B

Fig. 4.7 Transfer Characteristics

The highest saturation current for the first device stands at 0.54A/mm at V_{DS} = 6V whereas the maximum saturation current for the proposed device stands at 0.95A/mm at V_{DS} = 6V. The higher saturation current in transfer characteristics inhibits inefficient breakdown and aids in the achievement of a higher breakdown voltage.

4.2.6 Transconductance



(a) Device A (b) Device B

Fig. 4.8 Transconductance

The transconductance (g_m) variation with V_{GS} for both the devices is displayed in Fig. 4.8. An AC Simulation is performed for the device to obtain the transconductance which is plotted for drain voltages varying from +2V to +6V while the gate voltage is swept from 0V to+10V. The maximum g_m of 275 S/mm for the first device is reached at V_{DS} = 6V whereas the maximum g_m of 500 S/mm for the second device is reached at V_{DS} = 6V. The β-Ga_2O_3 buffer helped in having a higher transconductance which is crucial as this ensures the second device gives a higher gain while keeping all the other parameters constant. Also, higher transconductance ensures the device can be operated at higher frequencies improving the switching speed of the device tremendously.

4.2.7 Drain Leakage Current

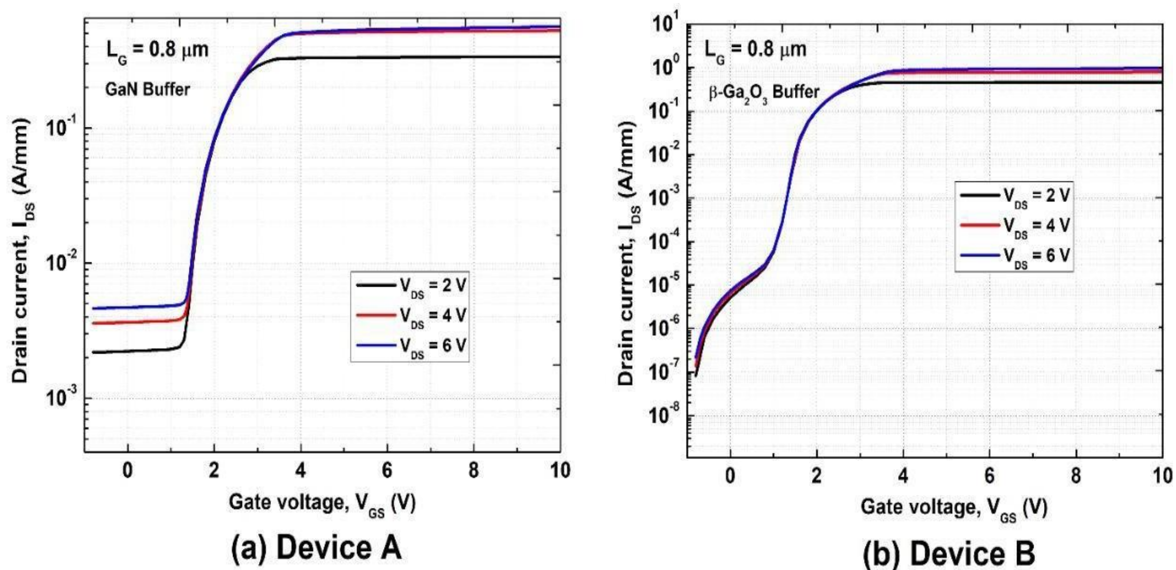


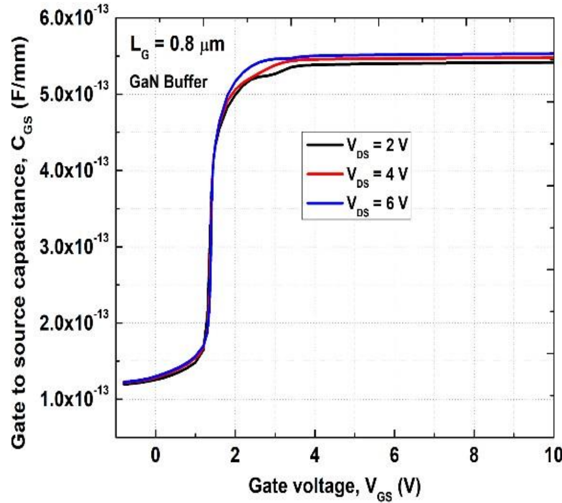
Fig. 4.9 Drain Leakage Current

The Drain leakage current of both the devices with gate length L_g = 0.8µm can be seen in Fig. 4.9. These are simulated when the device is in off state, and the gate voltage is swept from 0V to +10V for drain voltages carrying from +2V to +6V with a step size of 2V. It is evident that the drain leakage current of the proposed device with β-Ga_2O_3 buffer is less than the existing device with GaN buffer by a magnitude of 10^4. This is very important because a lesser leakage current means a longer battery life as there won't be much power leakage when the device is switched off. Also, the I_{on} to I_{off} ratio in the first device is about 10^3 whereas the I_{on} to I_{off} ratio

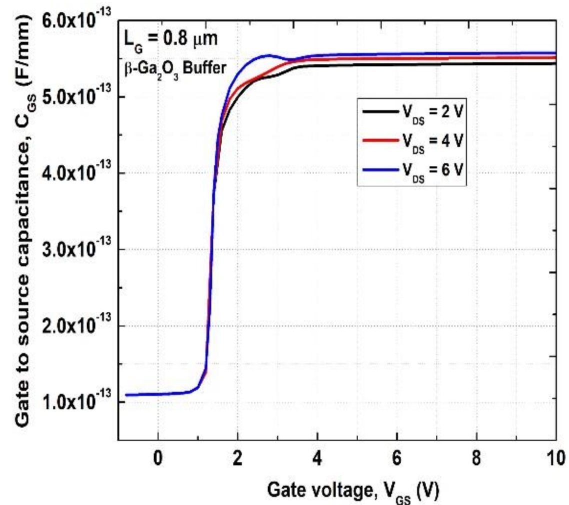
for the second device is 10^{7}. This higher I_{on} to I_{off} ratio enables the device to be operated at much higher frequencies.

4.2.8 Gate Capacitances

a) Gate to Source Capacitance



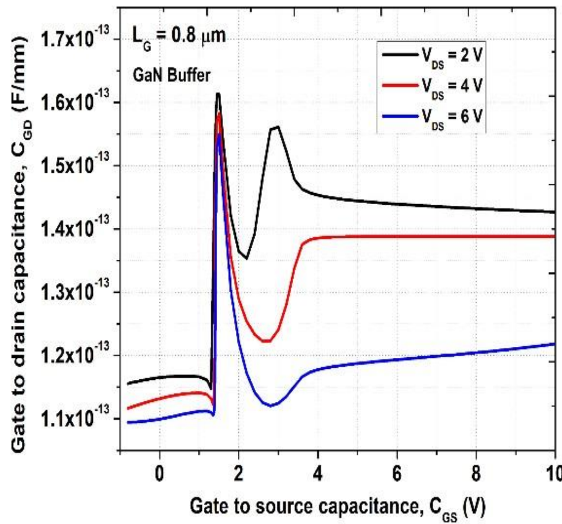
(a) Device A



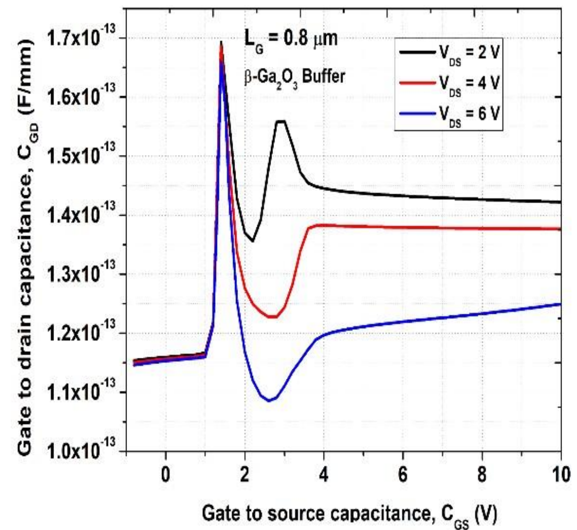
(b) Device B

Fig. 4.10 Gate to Source Capacitance, C_{GS}

b) Gate to Drain Capacitance



(a) Device A



(b) Device B

Fig. 4.11 Gate to Drain Capacitance, C_{GD}

The variation of Gate-Source Capacitance (C_{GS}) and Gate-Drain Capacitance (C_{DS}) is obtained for the sweep of gate voltage (V_{GS}) between 0V to +10V at V_{DS} varying between +2V to +6V with a step size of +2V can be seen in Fig. 4.10 and Fig. 4.11. There isn't much difference in the Capacitances as there are no field plates in either device, hence resulting in somewhat

similar capacitances. The maximum Gate-Source Capacitance (C_{GS}) in both the devices can be seen as $5.5x10^{-13}$ F/mm for a V_{DS} of 6V. Similarly, the maximum Gate-Drain Capacitance (C_{DS}) for both devices are $1.65x10^{-13}$ F/mm. Lower parasitic capacitances is preferable as that reduces switching delay as charge and discharge rate of capacitances reduces with lower capacitances.

4.2.9 Breakdown Voltage

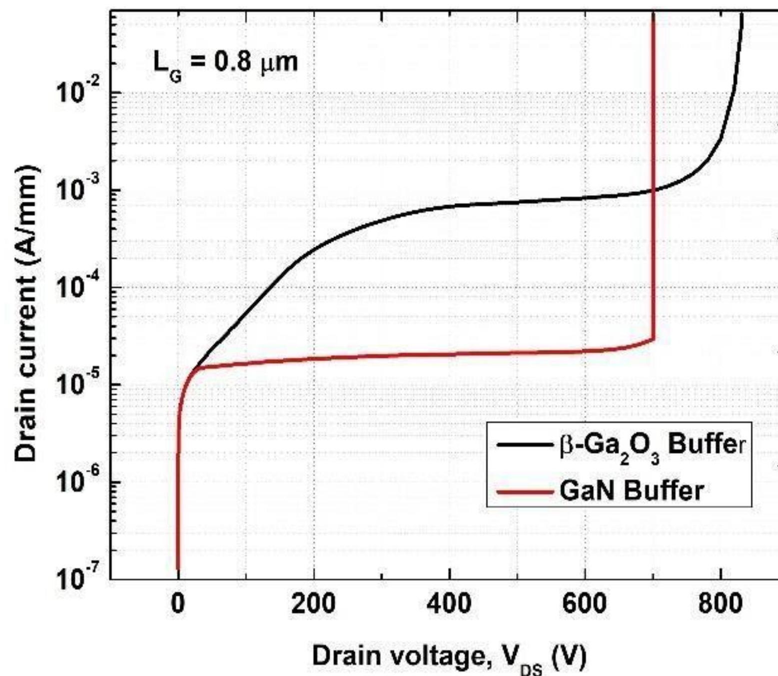


Fig. 4.12 Breakdown Voltage

A 750V off stage dielectric breakdown voltage of GaN buffer together with a switched off state breakdown voltage of 800V of β-Ga_2O_3 devices is determined by adjusting the Drain to Source Voltage as illustrated in Fig. 4.12. First the channel is entirely drained by providing negative bias towards the Gate-Source voltage so that ideally no current goes through transistor, then just a Drain-Source voltage sweep from 0 until breakdown occurs. Owing towards the depleted channel, it's current stays constant for a lengthy period of time until Catastrophic collapse happens. The increasing electromagnetic field between both the drain & gate regions generates a rise of breakdown voltage for second device having greater current. The two primary breakdown processes in HEMT systems are gate coupled breakdown & bulk associated breakdown. The major cause behind gate associated breakdowns is gate to drain leakage current. It is due to contaminants or flaws that generate a surface conducting channel. A Si3N4 sheath is utilized to decrease gate-drain leakage. It reduces the crest electromagnetic field just at gate's terminal's drain edge, boosting the device's dielectric breakdown voltage.

The bulk-related breakdown, was induced by a vertically leakage current between both the bulk area and the drain. It may be decreased by utilizing a strong AlGaN buffer layer.

4.2.10 Gate Switching Delay

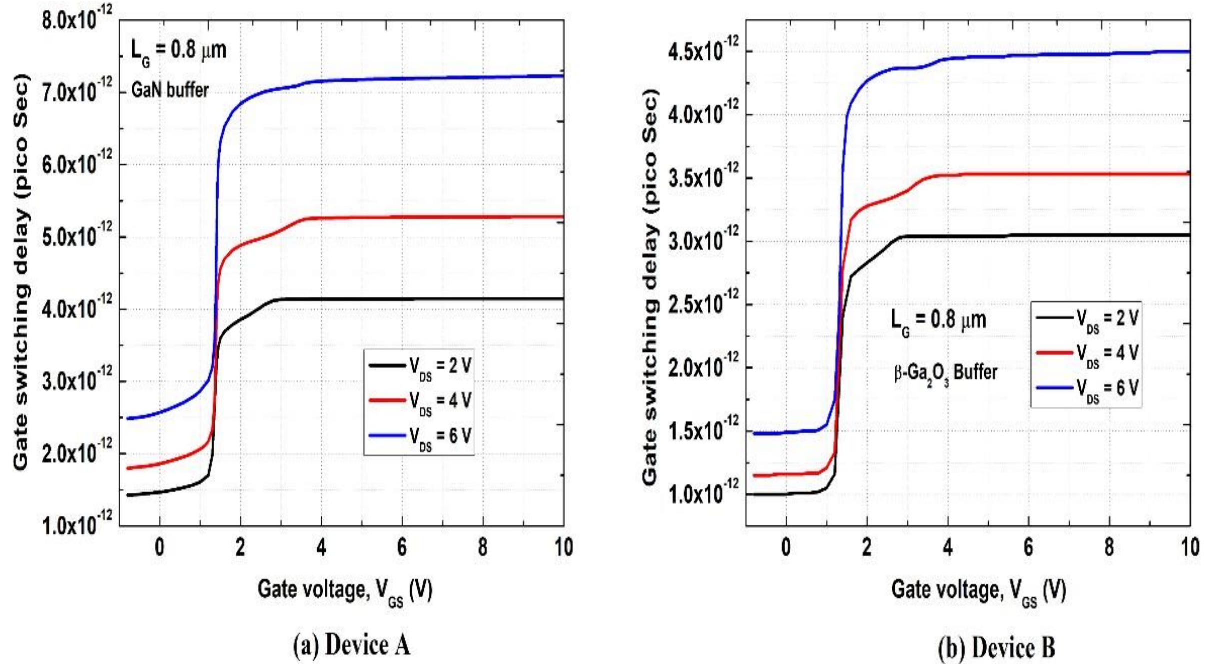


Fig. 4.13 Gate Switching Delay

The switching delay of both the devices can be seen in Fig 4.13. It is a key parameter to consider for high power switching applications and is calculated by:

$$\tau = R_{ON}.C_G \tag{4.3}$$

where,

$$R_{ON} = V_{DS}/I_{DS} \tag{4.4}$$

$$C_G = C_{GS} + C_{GD} \tag{4.5}$$

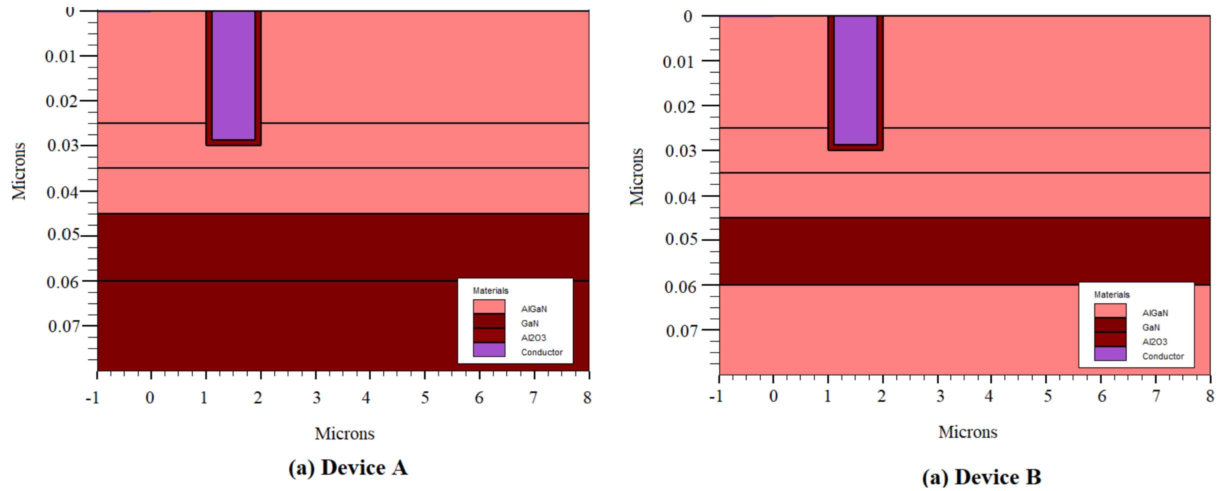
The HEMT's switching latency is depending on how rapidly the device switches on and off. The gate capacitance starts charging to its highest value during off to on state, but it begins discharging of its maximum point during on to off state. Energy loss in high-power switching devices are largely caused by parasitic capacitances of HEMTs.

Here, from the simulated outputs we can infer that the proposed device results in a very low gate switching delay of 4.5ps against the switching delay of 7.5ps for the existing GaN buffer device for a V_{DS} = 6V.

CHAPTER 5
A NORMALLY- OFF GAN METAL INSULATOR SEMICONDUCTOR FIELD EFFECT TRANSISTOR

In this chapter we discuss the second device, which is a GaN MISFET with a Gate of length 0.8µm. Once knowing about the device structure and composition we will check various parameters which are needed to know whether the proposed device is more efficient and reliable than already available devices in the market.

5.1 STRUCTURE



(a) Device A (a) Device B

Fig 5.1 Normally-off GaN MISHEMT with GaN and β-Ga_2O_3 as buffer

The vertical cross section view of MISHEMT with GaN Buffer as back gate and with a β-Ga_2O_3 buffer are seen in Fig 5.1. Instead of p-GaN as the gate, Al_2O_3 is used as the gate in this device. The total length of the device stands at 9µm. The length of Source and Drain is 1µm. The gate length is 0.8µm and the distance between Source and Gate is 1µm whereas the distance between Gate and Drain is 5µm. Here the lengths of Source and Drain is kept as 0 µm making the Source and Drain as thin as possible. However, the length of Al_2O_3 Gate is taken as 0.029µm. In Device A, GaN Buffer is used as the back gate followed by the substrate which is composed of GaN. Following this, three layers of $Al_{0.15}Ga_{0.85}N$ i.e., it has 15% Aluminum Nitride(AlN) and 85% Gallium Nitride (GaN).

In Device B, AlGaN buffer is used as the back gate followed by the substrate which is a layer of GaN. The composition of the AlGaN used in back gate is 7% Aluminum Nitride (AlN) and

93% Gallium Nitride (GaN) i.e., $Al_{0.07}Ga_{0.93}N$. The substrate is followed by three layers of AlGaN whose compositions are $Al_{0.15}Ga_{0.85}N$, $Al_{0.07}Ga_{0.93}N$ and $Al_{0.25}Ga_{0.75}N$.

5.2 RESULTS AND DISCUSSIONS

Below are the 10 key parameters that we considered checking the efficiency and reliability of the device we proposed.

5.2.1 Band Diagram

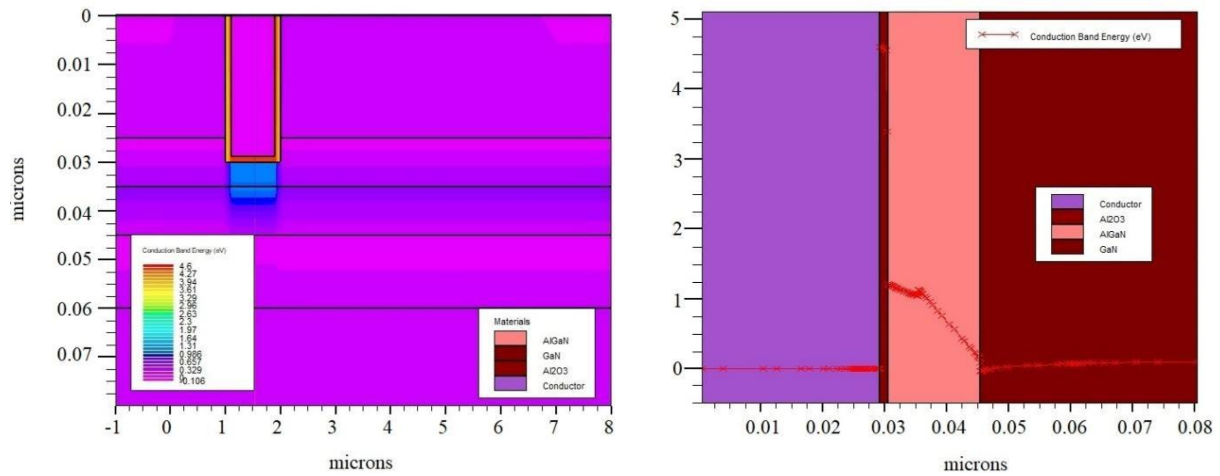


Fig 5.2(a) Band Diagram of GaN Buffer

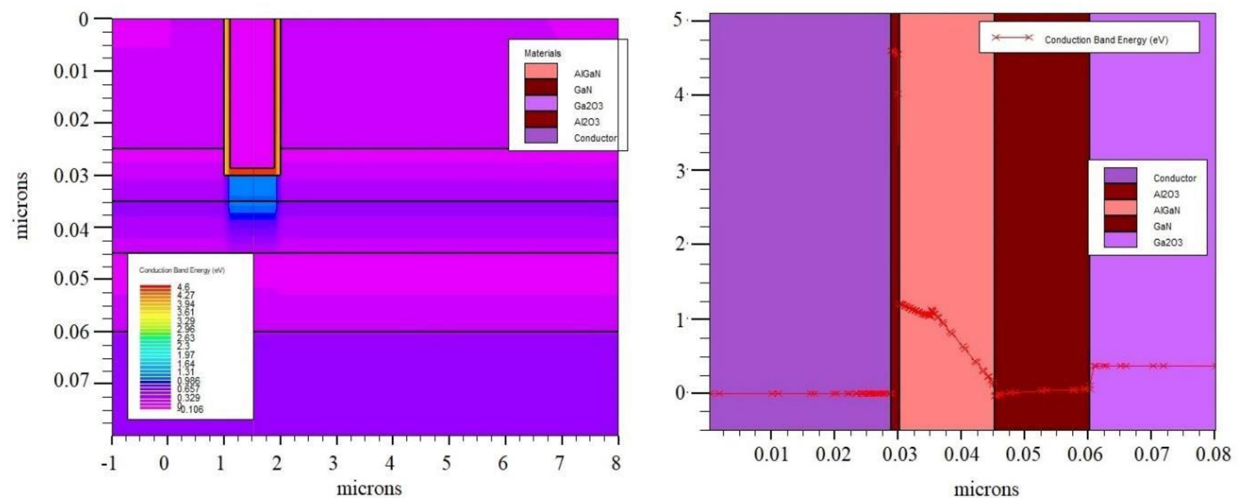


Fig 5.2(b) Band Diagram of β-Ga_2O_3 Buffer

The Band Diagram of the standard available device is compared against the proposed device. A clear 2DEG well is formed in the proposed device creating a well/barrier where electrons are confined. This ensures that there isn't any need for external polarization as there will be an internal polarization due to the high concentration of electrons in the well. We can also see that the difference between Valence Band and Conduction Band is higher in the

proposed device which makes the device tolerate higher electric fields which ensures the proposed device be operated at higher breakdown voltages.

5.2.2 Interface Charge

The AlN/β-Ga2O3 heterostructure's interface charge details are shown in Figure 5.3. The suggested heterostructure has an interface charge density (n_s) of 8.0×10^{12} cm^2 compared to the GaN Buffer device which has an interface charge density (n_s) of 1.0×10^{12} cm^2.

As shown in Eq. (5.1), the spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pz}) of various materials can be used to represent the polarization-induced sheet charge density (Δσ) at the heterojunction interface.

$$\Delta\sigma = -\Delta P = P_{sp}^{(sub)} - [P_{sp}^{epi} + P_{pz}^{(epi)}] \quad (5.1)$$

The piezoelectric polarization can be represented as

$$P_{PZ}^{(epi)} = 2[e_{31}^{(epi)} - e_{33}^{(epi)} \frac{C_{13}^{(epi)}}{C_{33}^{(epi)}}] \times \frac{a^{(epi)} - a^{(sub)}}{a^{(epi)}} \quad (5.2)$$

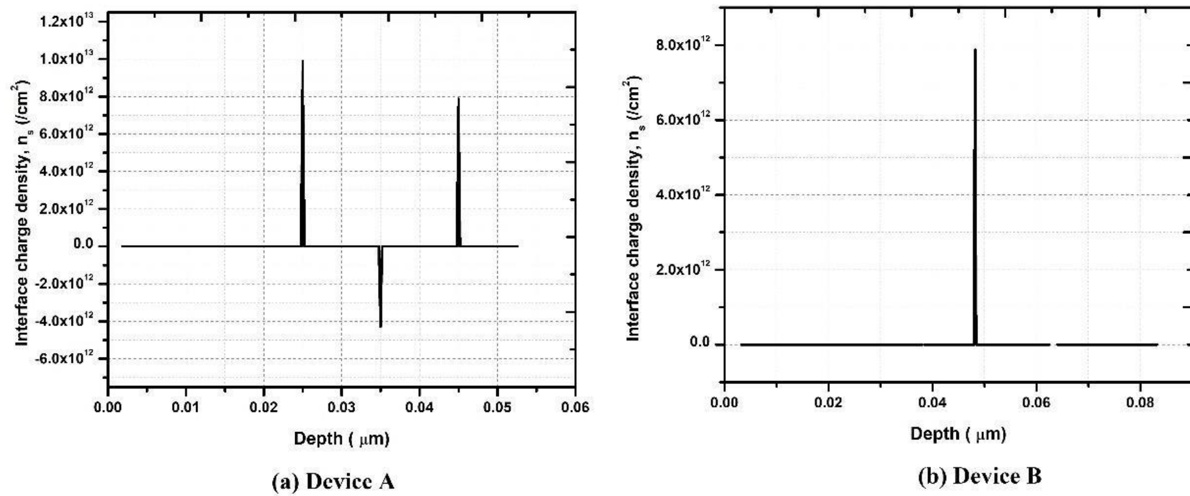


Fig 5.3 Interface Charge

5.2.3 Electron and Hole Concentration

Fig 5.4(a) and Fig 5.4(b) shows TCAD simulation of the Electron and Hole concentration of GaN buffer device for three different Drain-Source Voltage (V_{DS}) , which are +2V, +4V and +6V respectively.

Similarly, the TCAD simulation of Electron and Hole concentration for the proposed device with β-Ga_2O_3 buffer is seen in Fig 5.5(a) and Fig 5.5(b) for the same Drain to Source Voltages.

a. GaN Buffer

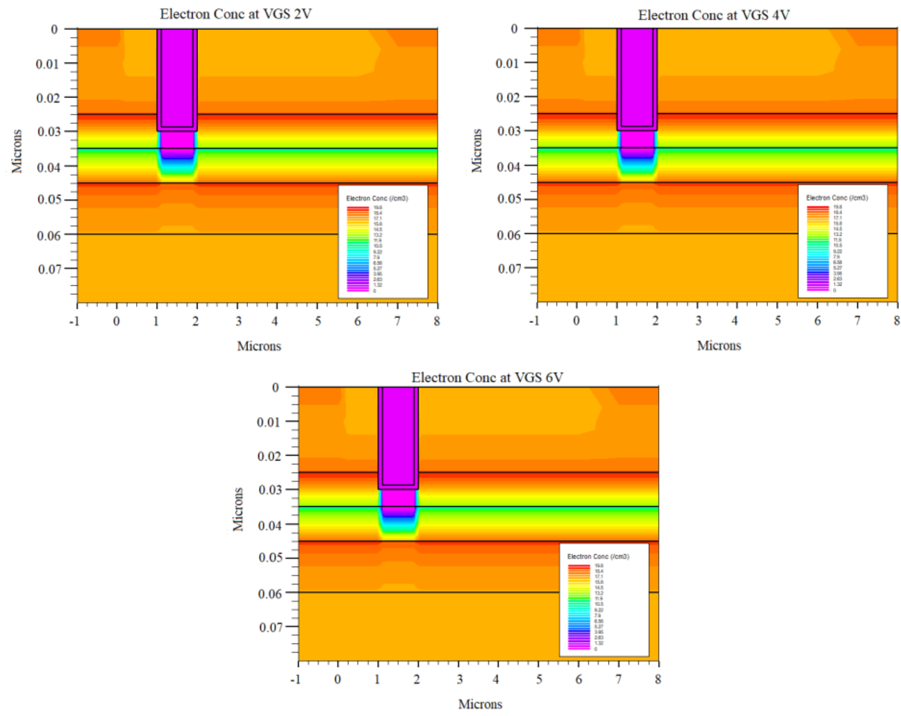


Fig 5.4(a) Electron Concentration of different V_{DS} levels

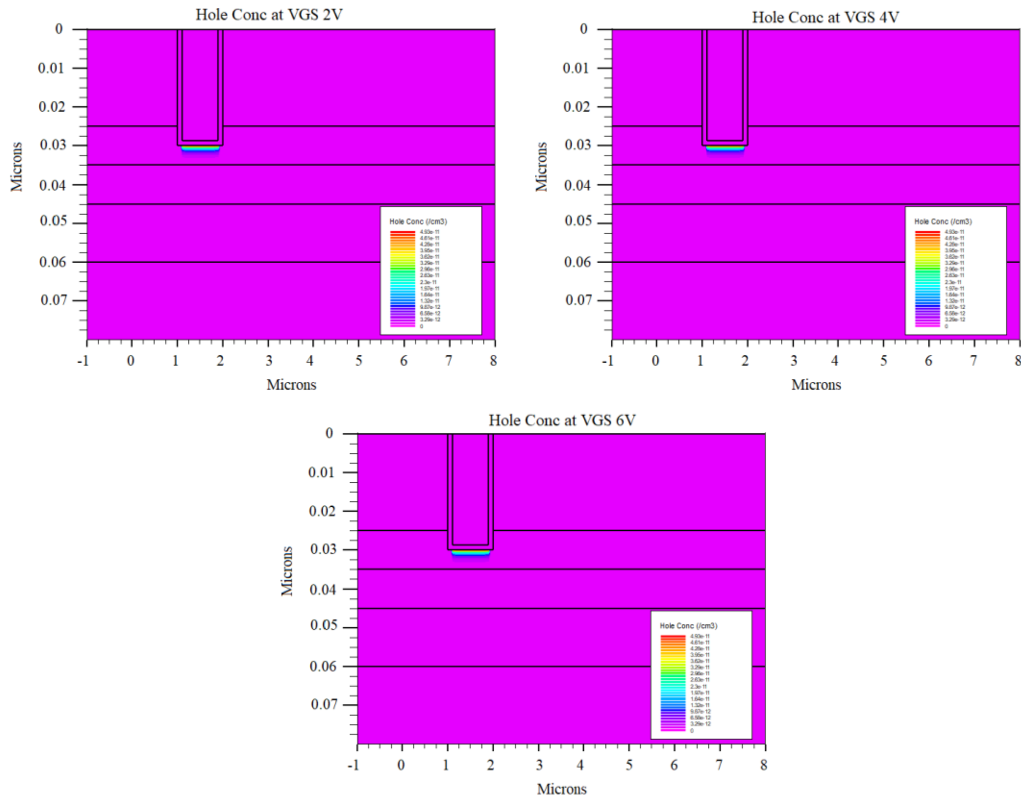


Fig 5.4(b) Hole Concentration at different V_{DS} levels

b. β-Ga_2O_3 Buffer

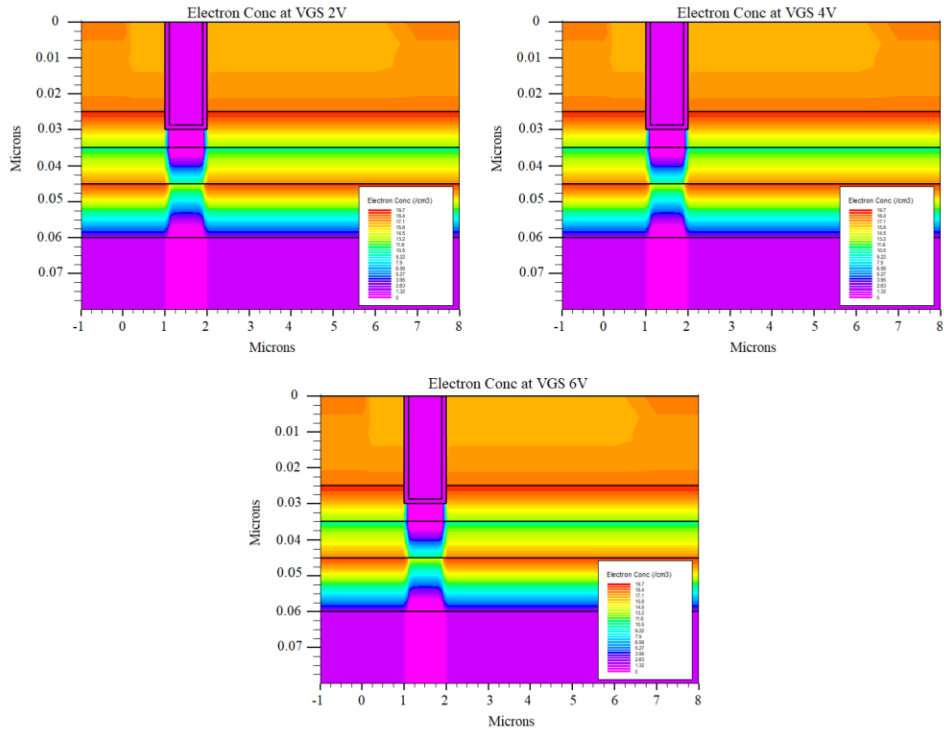


Fig 5.5(a) Electron Concentration of different V_{DS} levels

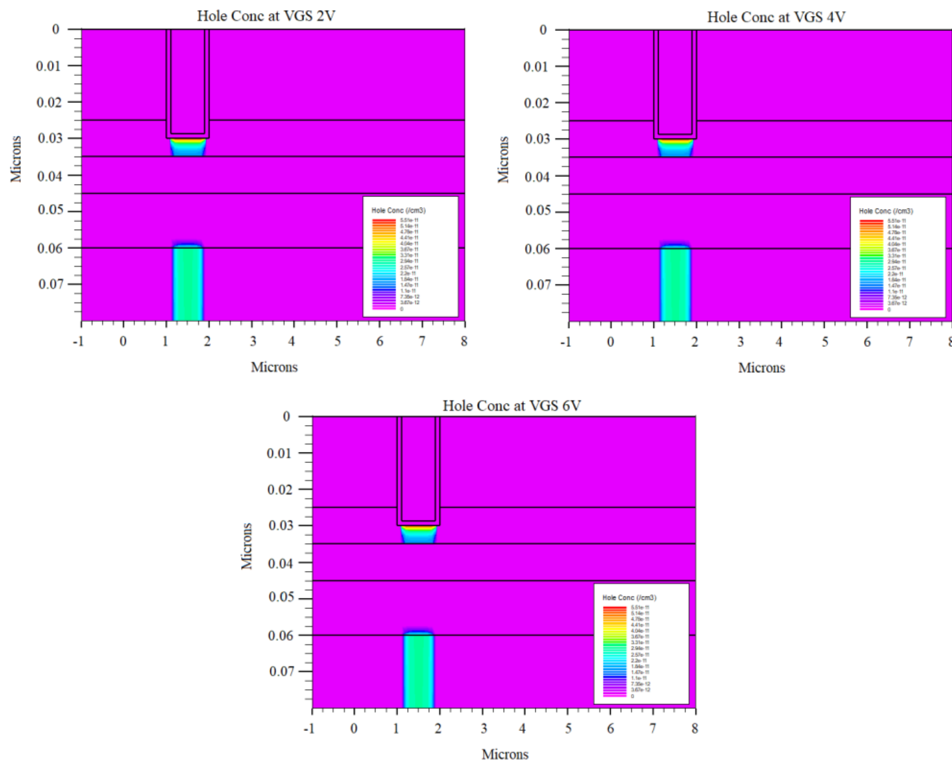


Fig 5.5(b) Hole Concentration at different V_{DS} levels

5.2.4 V-I Characteristics

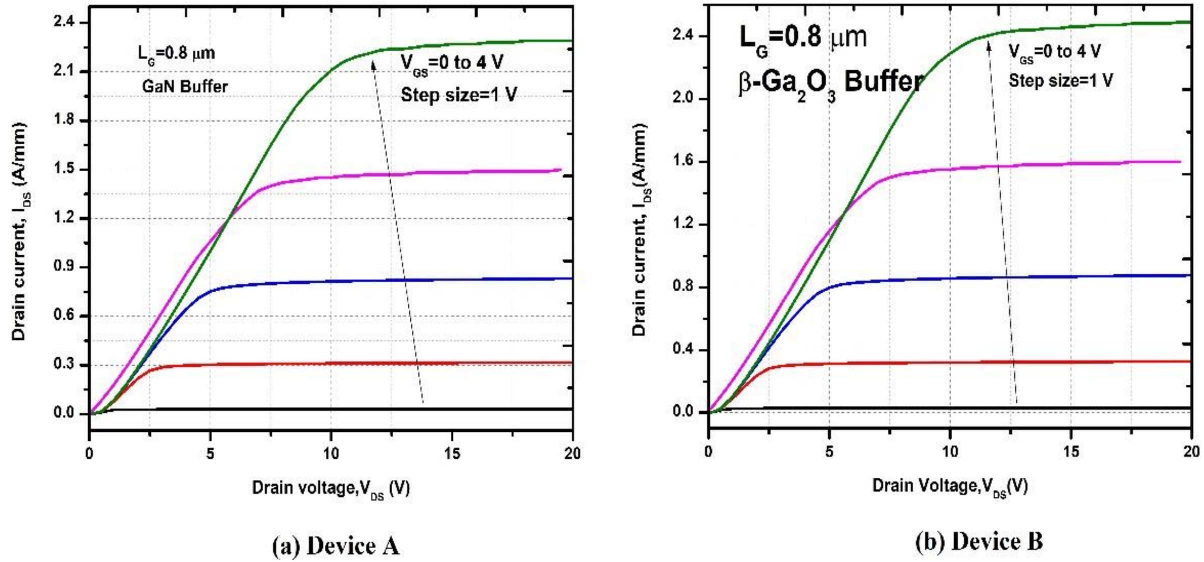
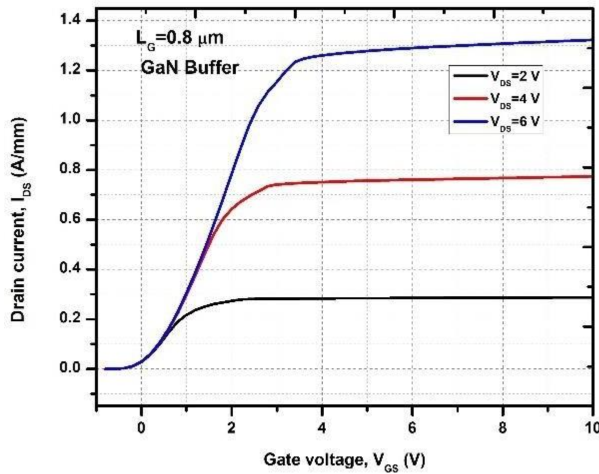


Fig 5.6 V-I Characteristics

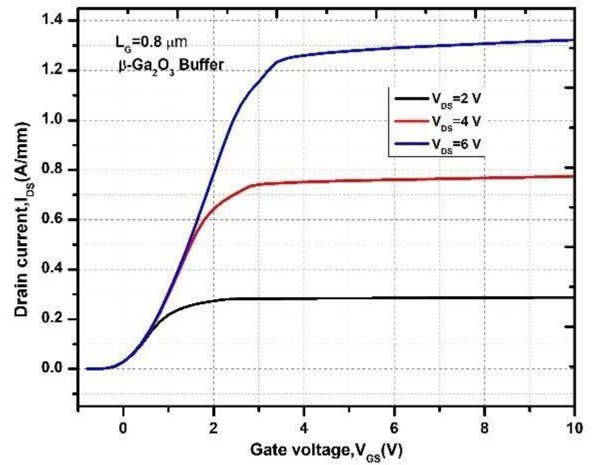
This figure shows the V-I characteristics of the existing device and the proposed device. The V-I characteristics are run for various Gate voltages varying from 0V to 4V with a step size of 1V. The drain voltage is swept from 0V to 20V. The respective drain currents for each gate voltage are plotted against the drain voltage for a device of gate length, L_g=0.8μm. The maximum current saturation is 2.23A/mm for the first device whereas it is 2.45A/mm in the case of the second device. We can see that the saturation currents of the second device are higher than the first device for same gate voltages which is due to the higher concentration of 2DEG because of the confined electrons in the well. This also means that the second device will deliver more output power comparatively due to higher output current for same voltages.

5.2.5 Transfer Characteristics

The simulation results for transfer characteristics of the existing device and proposed device are shown in Fig. 5.7. The transfer characteristics show the effect on output (I_{DS}) for varying input (V_{GS}). The drain voltages vary from +2V to +6V with a step size of 2V and the gate voltage is swept from 0V to +10V and the respective drain current is plotted for each drain voltage. The highest saturation current for both the devices stands at 1.32A/mm for a V_{DS} = 6V. The higher saturation current in transfer characteristics inhibits inefficient breakdown and aids in the achievement of a higher breakdown voltage.



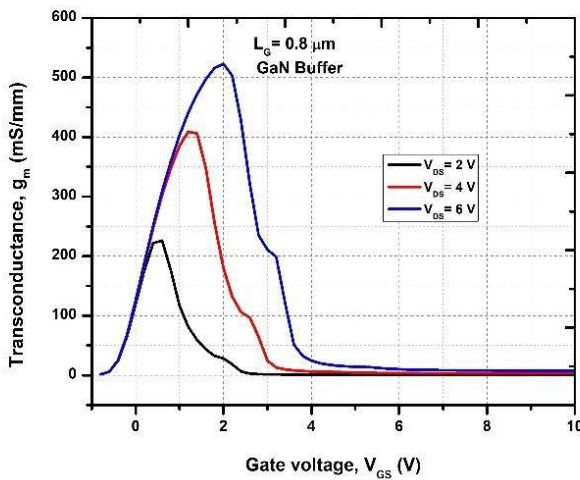
(a) Device A



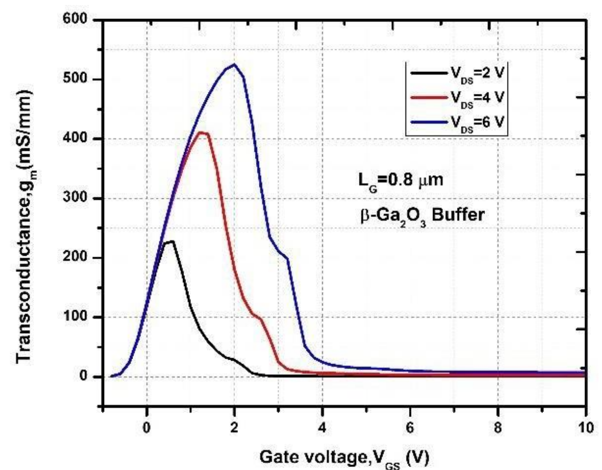
(b) Device B

Fig 5.7 Transfer Characteristics

5.2.6 Transconductance



(a) Device A



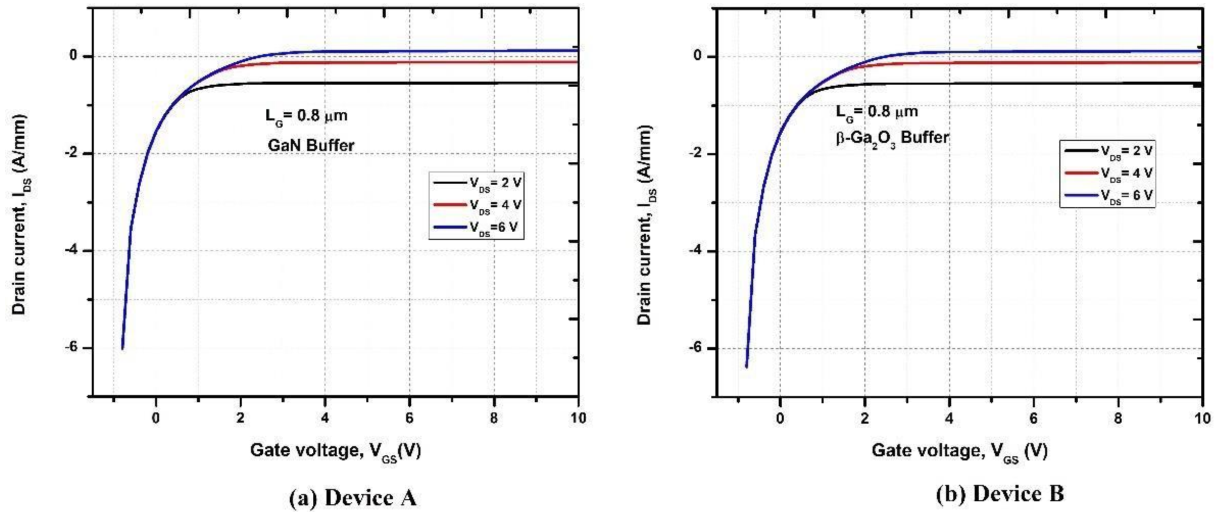
(b) Device B

Fig 5.8 Transconductance

The transconductance (g_m) variation with V_{GS} for both the devices is displayed in Fig. 3.8. An AC Simulation is performed for the device to obtain the transconductance which is plotted for drain voltages varying from +2V to +6V with a step size of +2V while the gate voltage is swept from 0V to+10V. The maximum g_m of 520 S/mm for both the devices is reached for a V_{DS} = 6V. The β-Ga_2O_3 buffer helps in having a better transconductance which is crucial as this ensures the second device gives a higher gain while keeping all the other

parameters constant. Also, higher transconductance ensures the device can be operated at higher frequencies improving the switching speed of the device tremendously.

5.2.7 Drain Leakage Current



(a) Device A **(b) Device B**

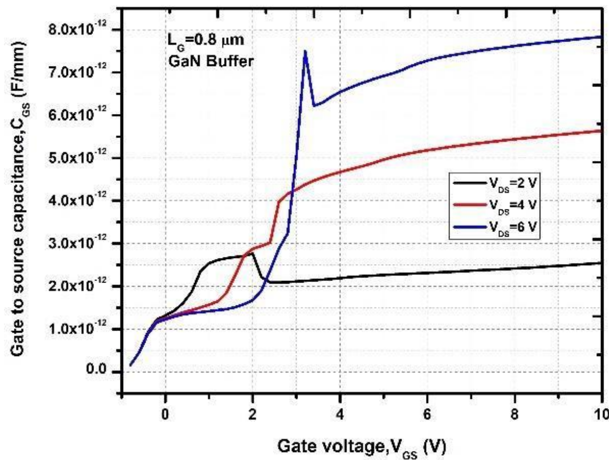
Fig 5.9 Drain Leakage Current

The Drain leakage current of both the devices with gate length $L_g = 0.8\mu m$ can be seen in Fig. 5.9. These are simulated when the device is in off state, and the gate voltage is swept from 0V to +10V for drain voltages carrying from +2V to +6V with a step size of 2V. This is very important because a lesser leakage current means a longer battery life as there won't be much power leakage when the device is switched off. Also, the I_{on} to I_{off} ratio in both the devices is high. This higher I_{on} to I_{off} ratio enables the device to be operated at much higher frequencies.

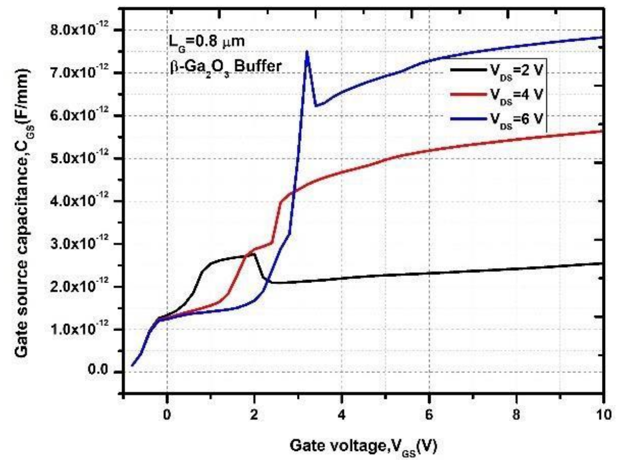
5.2.8 Gate Capacitances

The variation of Gate-Source Capacitance (C_{GS}) and Gate-Drain Capacitance (C_{DS}) is obtained for the sweep of gate voltage (V_{GS}) between 0V to +10V at V_{DS} varying between +2V to +6V with a step size of +2V can be seen in Fig. 5.10 and Fig. 5.11. There isn't much difference in the Capacitances as there are no field plates in either device, hence resulting in somewhat similar capacitances. The maximum Gate-Source Capacitance (C_{GS}) in both the devices can be seen as $7.8x10^{-12}$ F/mm for a V_{DS} of 6V. Similarly, the maximum Gate-Drain Capacitance (C_{DS}) for both devices are $2.25x10^{-12}$ F/mm. Having lower parasitic capacitances is preferable because then the switching delay would reduce as the time to charge and discharge the capacitances reduces with lower capacitances.

a) Gate to Source Capacitance



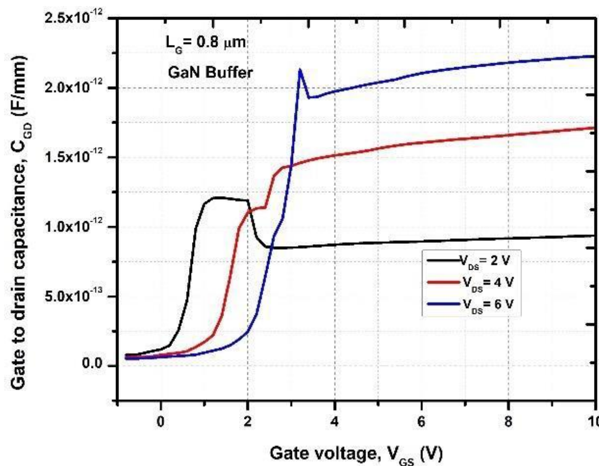
(a) Device A



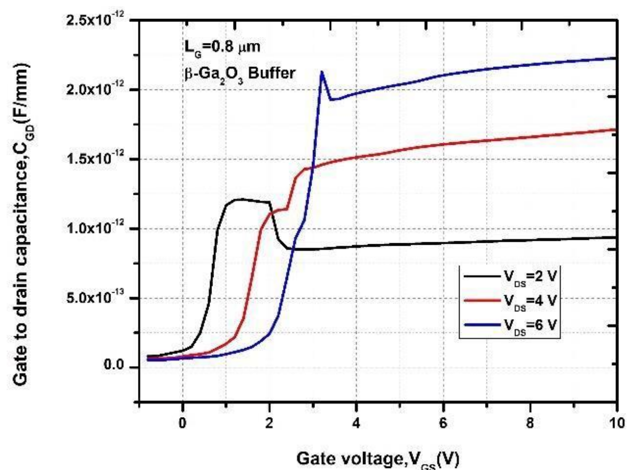
(b) Device B

Fig 5.10 Gate to Source Capacitance, C_{GS}

b) Gate to Drain Capacitance



(a) Device A

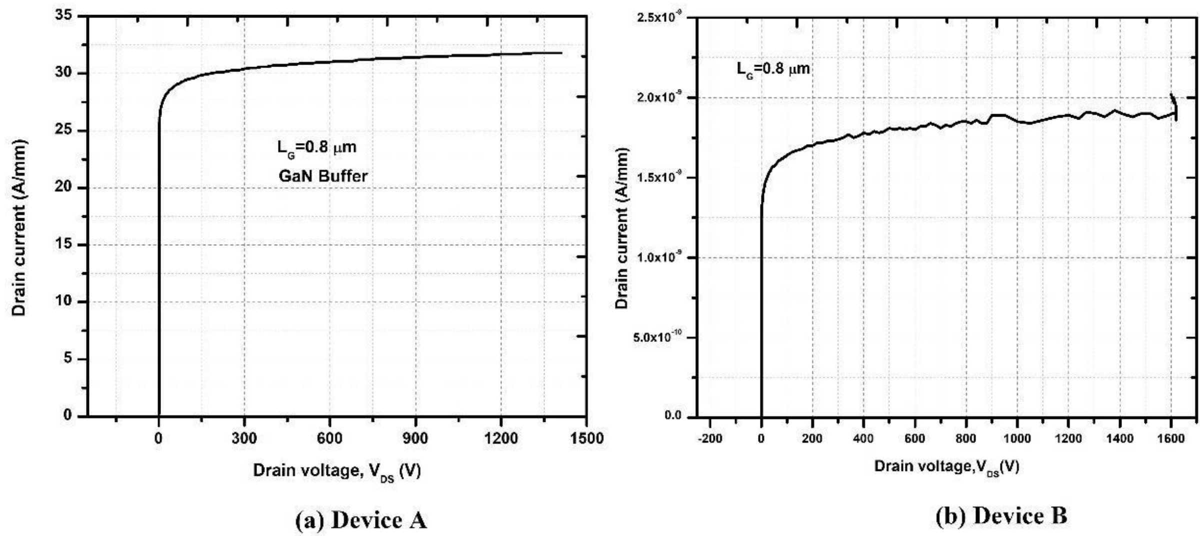


(b) Device B

Fig 5.11 Gate to Drain Capacitance, C_{GD}

5.2.9 Breakdown Voltage

A 1400V off state breakdown voltage for GaN buffer and an off-state breakdown voltage of 1600V for β-Ga_2O_3 device is measured by varying the Drain-Source Voltage as shown in Fig. 5.12. Initially the channel is completely depleted by applying negative bias to the Gate-Source voltage such that ideally no current passes through the device, then a Drain-Source voltage is swept from 0 till breakdown occurs. Due to the depleted channel, the current remains constant for a long period of time until Avalanche breakdown occurs.



(a) Device A

(b) Device B

Fig 5.12 Breakdown Voltage

The increased electric field between the drain and gate regions causes the increase in breakdown voltage for the second device with higher current. The two basic breakdown mechanisms in HEMT devices are gate associated breakdown and bulk associated breakdown. The principal cause of gate-associated breakdown is gate-drain leakage current. Using Al_2O_3 as the gate reduces the crest electric field at the drain edge of the gate terminal, increasing the device's breakdown voltage. The bulk-related breakdown, on the other hand, is caused by a vertical leakage current between the bulk region and the drain. It can be reduced by using a thick AlGaN buffer layer.

5.2.10 Gate Switching Delay

The switching delay of both the devices can be seen in Fig 5.13. It is a key parameter to consider for high power switching applications and is calculated by:

$$\tau = R_{ON}.C_G \quad (5.3)$$

where,

$$R_{ON} = V_{DS}/I_{DS} \quad (5.4)$$

$$C_G = C_{GS} + C_{GD} \quad (5.5)$$

The switching delay of a HEMT is determined by how rapidly the device turns on and off. The gate capacitance begins charging to its peak value during the off to on state, and it begins discharging from its peak value during the on to off state. Power losses in high-power switching circuits are mostly caused by the parasitic capacitances of HEMTs.

Based on the simulated outputs, we can conclude that both devices have a very low gate switching latency of 4.6ps for a V_{DS} = 6V.

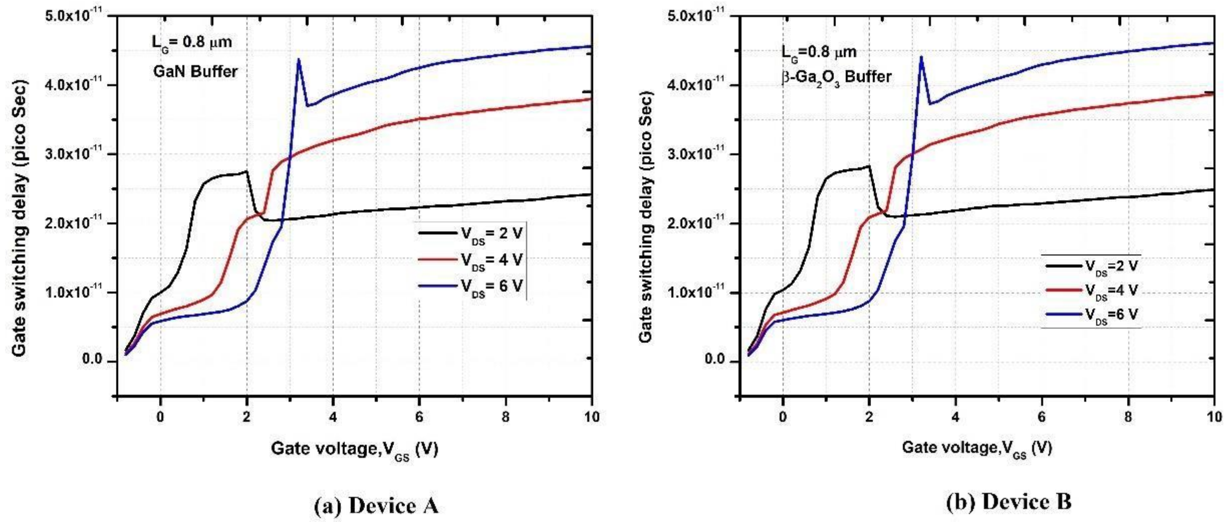


Fig 5.13 Gate Switching Delay

CONCLUSION

The Device having β-Ga_2O_3 as the back gate instead of using a simple GaN Buffer yielded better results for both the Normally off p-GaN gate device & Normally off GaN MISHEMT. The project successfully implemented the execution of two devices in which each device a comparison of an existing device with GaN as back gate is done with the same device having β-Ga_2O_3 as the back gate.

All the parameters which were considered for comparison yielded better results for the proposed device having β-Ga_2O_3 as the back gate. The most critical metric which we intended to enhance is indeed the dielectric breakdown voltage which was effectively done. The greater breakdown voltage permits us to operate our suggested device at larger input voltages without impacting the device. Additionally, higher voltages enable more power to be delivered with less loss across the same dimension (and weight) of copper wire. Aside from all this, increased voltages also aid in decreasing the charging time, produce lower current which decreases heat, enabling us to have smaller and less cumbersome wires, plus reduces the size of many other electric equipment. Other metrics such as the drain leakage current, transconductance, gate switching latency also improved which aids in fewer power consumption, running the device at higher frequencies and offer greater output power which is needed to operate the batteries in an Electric Vehicle.

FUTURE WORK

The ability of GaN systems to replace the Si for switching applications is a crucial area of research in the field of Device Physics. There are several future scope and improvements that can be considered in the field of GaN systems. Some of them are:

1) Although major progress has been achieved in recent years for the use of GaN systems in Electric Vehicles, the growth process is continuous research. Steady improvement has been achieved in increasing the breakdown hence the operating voltage, maximizing operating frequency, and decreasing the power loss. But many global automobile companies are investing a lot in Research and Development of the GaN systems in Electric Vehicles.
2) Currently all the Electric Cars are operating at 400V while the research is being conducted to have an 800V operating voltage. This will half the charging time, reduce the size of battery, and greatly improve the mileage of the car.
3) Existing GaN devices have restricted power handling capabilities. But, with 1200V GaN transistors down the road, the application may be expanded to incorporate more power & frequency over IGBTs, Si MOSFETs, & SiC semiconductors.
4) An EV's efficacy is also affected by effectiveness of its electronic power motor drive. When assessing a motor driver, both the inverters as well as the motor must be taken into consideration. Increasing motor drive efficiency decreases costs and heat needs, formulating new EVs more competitive versus ICE cars.
5) Although we were able to improve the breakdown voltage and saturation current for V-I characteristics for the second device, remaining parameters remained almost the same for both the back gates which can be improved.

The model improvements and future work listed above is to serve as motivation for future research in this area. GaN systems offer various advantages over the traditional Si based systems which made it a great alternative especially in the field of EV where better breakdown voltages, lower power and higher operating frequencies are crucial. Future research will be exploring the applications of GaN systems completely and making great use of it in various fields not just limited to Electric Vehicles.

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